

## Open-Q 835 $\mu$ SOM HW Device Specification

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# 1. INTRODUCTION

This document applies to the Open-Q 835  $\mu$ SOM. Technical specifications for other SOMs in the Intrinsic product line are covered under separate documents.

## 1.1 Purpose

The purpose of this document is to provide the technical specifications of the Intrinsic Open-Q 835  $\mu$ SOM.

## 1.2 Scope

This document covers the following information on the Open-Q 835  $\mu$ SOM:

- Electrical and mechanical specifications
- SOM pin-out
- Device handling and packaging
- Ordering information.

## 1.3 Intended Audience

This document is intended for users who wish to understand the technical specifications of the Intrinsic Open-Q 835  $\mu$ SOM.

## 1.4 Acronyms and Abbreviations

Acronym / Abbreviation	Definition
ANT	ANTenna
BAT, BATT	BATTery
BAM	Bus Access Manager
BLSP	BAM-based Low-Speed Peripheral
BOM	Bill Of Materials
BT	Blue Tooth
CLK	Clock
CPU	Central Processing Unit
CS	Chip Select
CSI	Camera Serial Interface
DSI	Display Serial Interface
EMI	Electro-Magnetic Interference
EN	ENable
ERM	Eccentric Rotating Mass
ESD	Electro-Static Discharge
GND	GrouND
GPIO	General Purpose I/O
GPS	Global Positioning System
HDMI	High Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
INT	INTerrupt
JTAG	Joint Test Action Group

Acronym / Abbreviation	Definition
LDO	Low Drop-Out
LRM	Linear Resonant Actuator
LTE	Long-Term Evolution
LPI	Low Power Island
MDP	Mobile Display Port
MI2S	Mobile Inter-IC Sound
MIC	MICrophone
MIPI	Mobile Industry Processor Interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
PCB	Printed Circuit Board
PCIE	Peripheral Component Interconnect Express
PWM	Pulse-Width Modulation
QUP	Qualcomm Universal Peripheral
RF	Radio Frequency
RX	Receive
SCL	Serial Clock
SDA	Serial DATA
SDC	Secure Digital Interface
SOM	System On Module
SPI	Serial Peripheral Interface
SSC	Snapdragon Sensor Core
TX	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UIM	User Interface Module
USB	Universal Serial Bus
WLAN	Wireless Local Area Network

## 1.5 Signal Name Suffix

Suffix	Definition
_N	Indicates that the signal is ACTIVE LOW
_P/N	Identifies the two signals comprising a differential pair

## 2. DOCUMENTS

This section lists any parent and supplementary documents for the Open-Q 835  $\mu$ SOM Device Specification. Unless stated otherwise, applicable documents supersede this document and reference documents provide background and supplementary information.

### 2.1 Applicable Documents

REFERENCE	AUTHOR	TITLE
A-1	Intrinsyc	Intrinsyc Purchase and Software License Agreement for the Open-Q 835 $\mu$ SOM

### 2.2 Reference Documents

Available at <http://tech.intrinsyc.com> (dev kit registration required).

REFERENCE	TITLE
R-1	Open-Q 835 $\mu$ SOM Development Kit – User Guide
R-2	Open-Q 835 $\mu$ SOM – Carrier Board Design Guide
R-3	Open-Q 835 $\mu$ SOM Schematics (SOM and Carrier)
R-4	Open-Q 835 $\mu$ SOM Modular Certification OEM Integrator Guide

### **3. SUMMARY OF FEATURES**

The Open-Q 835  $\mu$ SOM contains the core of the Snapdragon 835 architecture. Measuring in at 50mm x 25mm, the SOM is where all the processing occurs. It connects to a carrier board via three 100 pin Hirose DF40 connectors which allows essential power rails and signals to be exposed for supporting peripherals and interfaces on the platform.



### 3.1 SOM Block Diagram

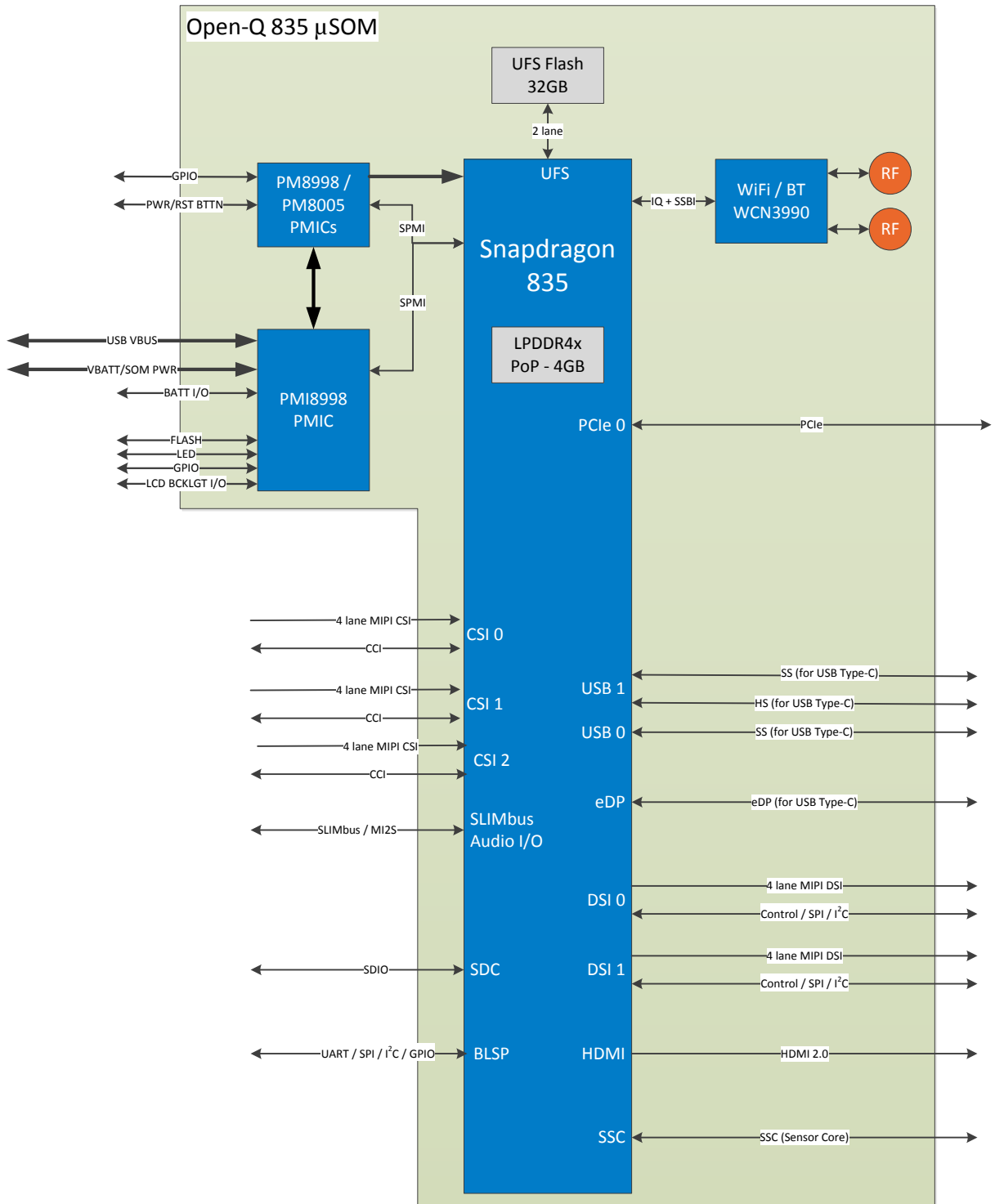


Figure 1 – Open-Q 835  $\mu$ SOM Block Diagram

## 3.2 SOM Technical Specifications

See the table below for the Open-Q 835  $\mu$ SOM technical specifications.

**Table 1 – Open-Q 835  $\mu$ SOM Technical Specifications**

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	APQ8098	Qualcomm® Snapdragon 835 Processor	Qualcomm® Kryo CPU, quad core, 64-bit ARM V8 compliant processor, 2.2GHz
	PMIC (PMI8998, PM8998, PM8005)	Qualcomm® PMIC, Companion PMIC for APQ8098 processor	NA
Memory	4GB LPDDR4	Memory POP	Up to 1866MHz LPDDR4 POP on CPU BGA chip. Supports via 4x16bit channels
	32 GB UFS	Primary Storage for platform. Mainly used for storing SW applications and user data etc.	Toshiba UFS on board. Can support up to 256GB
RF Connectivity	Wi-Fi 2.4 GHz/ 5GHz via WCN3990	Wi-Fi WCN3990 Wi-Fi + BT Combo Chip	802.11a/b/g/n/ac 2.4/5.0 GHz via WCN3990. Full 2x2 antenna configuration
	BT 2.4 GHz via WCN3990	Wi-Fi WCN3990 Wi-Fi + BT Combo Chip	Support Bluetooth 5 (LE 5.x + HS)
RF Interfaces (see section below)	WLAN / BT	2 antenna connectors on SOM for 2x2 MIMO Wi-Fi. Bluetooth uses one of the 2 antenna ports.	2 x U.FL, 50 ohm coaxial connectors
Multimedia	MIPI CSI	Three 4-lane MIPI CSI Camera interfaces	4-lane supporting MIPI CSI D-PHY v1.2
	MIPI DSI	Two 4-lane MIPI DSI Display interfaces	Supporting MIPI DSI D-PHY v1.2
	HDMI	One HDMI video output interface	HDMI v2.0a
Audio Interfaces	MI2S	Multiple Audio ports are routed out and configurable for MI2S, PCM, or GPIO	
	SLIMBUS	2 bit SLIMBUS port	Support for external audio codec
Digital Interfaces	USB	One USB 3.1 which can support Type-C with Display Port	USB3.1 & USB2.0
	PCIe	One PCI-SIG PCIe interface	v2.1 PHY v2.1 controller
	SDIO	One 4-bit Secure Digital interface	SD v3.0, dual voltage interface
	GPIO / I2C / SPI / UART	Configurable IO	Configurable IO exposed as GPIO or BLSP ports, giving GPIO, I2C, SPI, and UART connections options.
Connectors	3x 100-pin board to board connectors	3x Hirose 100-pin DF40C header connectors	300 pins total for connection to carrier board

## 4. I/O DEFINITIONS

### 4.1 Location of Major Components

The figures below identify the major components and connectors found on the Open-Q 835  $\mu$ SOM top and bottom sides.

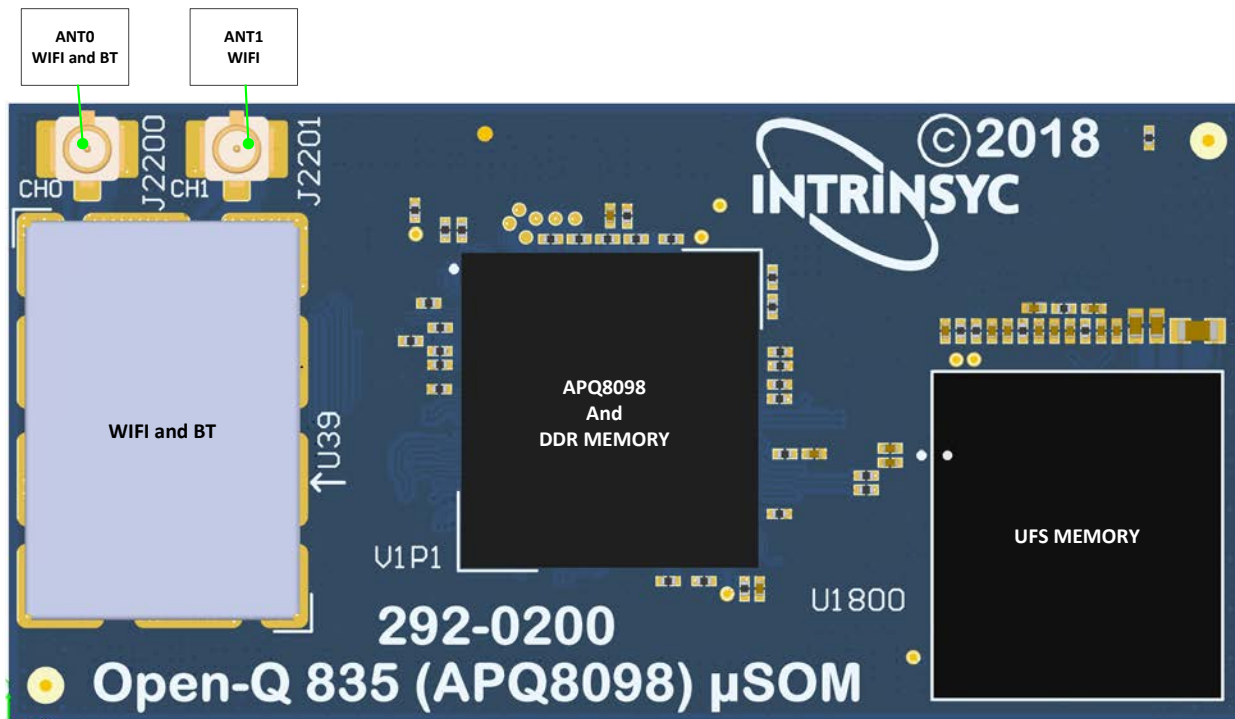


Figure 2 – Open-Q 835  $\mu$ SOM Top View

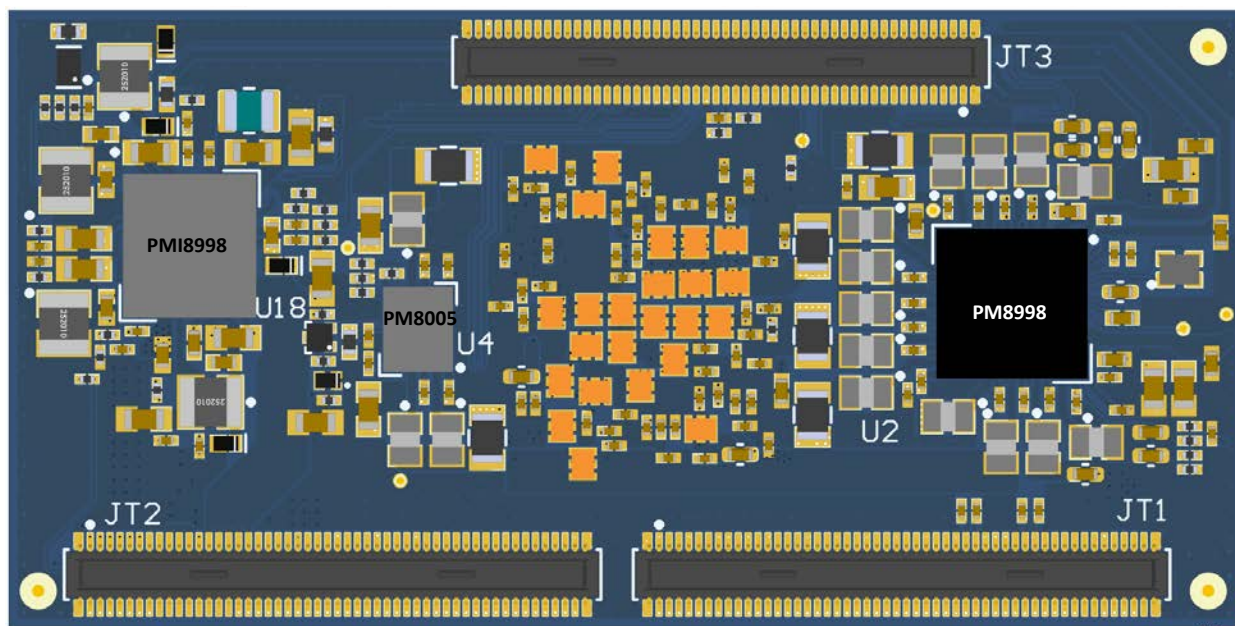


Figure 3 – Open-Q 835  $\mu$ SOM Bottom View

The SOM mating connectors JT1, JT2, and JT3 are located on the bottom side of the SOM. The connector pin 1 locations are shown in the figure below (looking at bottom of SOM). Key dimensions are provided in later sections of this document.

The connectors are Hirose DF40C-100DP-0.4V(51). See section 6.3 for information on the available mating connectors.

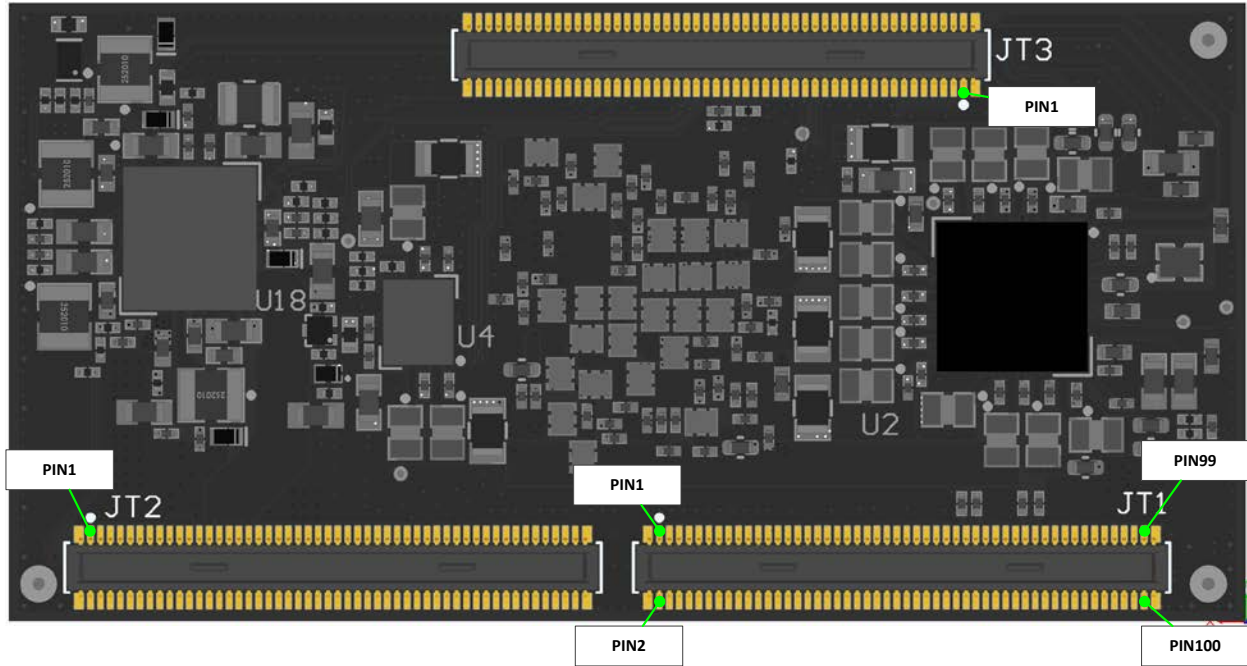


Figure 4 – Pin Locations of Board-to-Board Connectors

## 4.2 B2B Connector Signal Assignments

The following tables list the pin-outs of the three Open-Q 835  $\mu$ SOM board to board connectors. A more detailed description of the signal group functions can be found in document R-2 which provides background information for customers developing a custom Carrier Board for the Open-Q 835  $\mu$ SOM.

Note: the SOM schematic (document R-3) is the controlling document. In the event of pin-out difference(s) between this document and the SOM schematic, the SOM schematic shall take precedence.

Table 2 – B2B Connector JT1 Pin-outs

Pin #	JT1 Signal Name	Description
1	GND	Ground reference for design.
2	GND	Ground reference for design.
3	HDMI_TX0_N	HDMI transmit lane 0
4	HDMI_TX1_N	HDMI transmit lane 1
5	HDMI_TX0_P	HDMI transmit lane 0
6	HDMI_TX1_P	HDMI transmit lane 1
7	GND	Ground reference for design.

Pin #	JT1 Signal Name	Description
8	GND	Ground reference for design.
9	HDMI_TX2_N	HDMI transmit lane 2
10	HDMI_TCLK_N	HDMI differential clock pair
11	HDMI_TX2_P	HDMI transmit lane 2
12	HDMI_TCLK_P	HDMI differential clock pair
13	GND	Ground reference for design.
14	GND	Ground reference for design.
15	GND	Ground reference for design.
16	MIPI_CSI0_CLK_P	MIPI CSI clock differential pair
17	CCI_I2C_SDA0	CPU GPIO17
18	MIPI_CSI0_CLK_N	MIPI CSI clock differential pair
19	GND	Ground reference for design.
20	GND	Ground reference for design.
21	CCI_I2C_SDA1	CPU GPIO19
22	MIPI_CSI0_LANE3_P	MIPI CSI data lane3 differential pair
23	CAM_MCLK1	CPU GPIO14
24	MIPI_CSI0_LANE3_N	MIPI CSI data lane3 differential pair
25	CAM_MCLK2	CPU GPIO15
26	GND	Ground reference for design.
27	CCI_I2C_SCL0	CPU GPIO18
28	MIPI_CSI0_LANE2_P	MIPI CSI data lane2 differential pair
29	CCI_I2C_SCL1	CPU GPIO20
30	MIPI_CSI0_LANE2_N	MIPI CSI data lane2 differential pair
31	GND	Ground reference for design.
32	GND	Ground reference for design.
33	MIPI_CSI1_LANE1_P	MIPI CSI data lane1 differential pair
34	MIPI_CSI0_LANE1_P	MIPI CSI data lane1 differential pair
35	MIPI_CSI1_LANE1_N	MIPI CSI data lane1 differential pair
36	MIPI_CSI0_LANE1_N	MIPI CSI data lane1 differential pair
37	GND	Ground reference for design.
38	GND	Ground reference for design.
39	MIPI_CSI1_CLK_P	MIPI CSI clock differential pair
40	MIPI_CSI0_LANE0_P	MIPI CSI data lane0 differential pair
41	MIPI_CSI1_CLK_N	MIPI CSI clock differential pair
42	MIPI_CSI0_LANE0_N	MIPI CSI data lane0 differential pair
43	GND	Ground reference for design.
44	GND	Ground reference for design.
45	MIPI_CSI1_LANE0_N	MIPI CSI data lane0 differential pair
46	MIPI_CSI2_CLK_P	MIPI CSI clock differential pair
47	MIPI_CSI1_LANE0_P	MIPI CSI data lane0 differential pair

Pin #	JT1 Signal Name	Description
48	MIPI_CSI2_CLK_N	MIPI CSI clock differential pair
49	GND	Ground reference for design.
50	GND	Ground reference for design.
51	MIPI_CSI1_LANE2_P	MIPI CSI data lane2 differential pair
52	MIPI_CSI2_LANE0_P	MIPI CSI data lane0 differential pair
53	MIPI_CSI1_LANE2_N	MIPI CSI data lane2 differential pair
54	MIPI_CSI2_LANE0_N	MIPI CSI data lane0 differential pair
55	GND	Ground reference for design.
56	GND	Ground reference for design.
57	MIPI_CSI1_LANE3_P	MIPI CSI data lane3 differential pair
58	MIPI_CSI2_LANE3_P	MIPI CSI data lane3 differential pair
59	MIPI_CSI1_LANE3_N	MIPI CSI data lane3 differential pair
60	MIPI_CSI2_LANE3_N	MIPI CSI data lane3 differential pair
61	GND	Ground reference for design.
62	GND	Ground reference for design.
63	USB3_SS_TX0_C_P	USB super-speed port TX0 differential pair
64	MIPI_CSI2_LANE1_P	MIPI CSI data lane1 differential pair
65	USB3_SS_TX0_C_N	USB super-speed port TX0 differential pair
66	MIPI_CSI2_LANE1_N	MIPI CSI data lane1 differential pair
67	GND	Ground reference for design.
68	GND	Ground reference for design.
69	USB3_SS_RX0_P	USB super-speed port RX0 differential pair
70	MIPI_CSI2_LANE2_P	MIPI CSI data lane2 differential pair
71	USB3_SS_RX0_N	USB super-speed port RX0 differential pair
72	MIPI_CSI2_LANE2_N	MIPI CSI data lane2 differential pair
73	GND	Ground reference for design.
74	GND	Ground reference for design.
75	USB3_SS_TX1_C_P	USB super-speed port TX1 differential pair
76	LPG_WLED	PMI8998 GPIO 8
77	USB3_SS_TX1_C_N	USB super-speed port TX1 differential pair
78	KEY_VOLP_N	PM8998 GPIO6
79	GND	Ground reference for design.
80	GND	Ground reference for design.
81	USB3_SS_RX1_P	USB super-speed port RX1 differential pair
82	PCIE_REFCLK_N	PCIe CLK differential pair

Pin #	JT1 Signal Name	Description
83	USB3_SS_RX1_N	USB super-speed port RX1 differential pair
84	PCIE_REFCLK_P	PCIe CLK differential pair
85	GND	Ground reference for design.
86	GND	Ground reference for design.
87	AUX_P	USB Type-C SBU1/2 (or EDP_AUX) for USB Type-C alt Display Port mode function
88	PCIE_RX_P	PCIe RX differential pair
89	AUX_N	USB Type-C SBU1/2 (or EDP_AUX) for USB Type-C alt Display Port mode function
90	PCIE_RX_N	PCIe RX differential pair
91	GND	Ground reference for design.
92	GND	Ground reference for design.
93	CAM_MCLK3	CPU GPIO16
94	PCIE_TX_N	PCIe TX differential pair
95	VREG_LVS2A_1P8	Low voltage switch L2 Default voltage = 1.80V Maximum Current = 100mA
96	PCIE_TX_P	PCIe TX differential pair
97	VREG_LVS1A_1P8	Low voltage switch L1 Default voltage = 1.80V Maximum Current = 300mA
98	GND	Ground reference for design.
99	CAM_MCLK0	CPU GPIO13
100	VREG_L22A_2P85	LDO linear regulator L22 Default voltage = 2.85V Maximum Current = 150mA

Table 3 – B2B Connector JT2 Pin-outs

Pin #	JT2 Signal Name	Description
1	VBATT_PWR	3.80-4.20VDC power input to SOM.
2	GND	Ground reference for design.
3	VBATT_PWR	See JT2 pin 1
4	GND	Ground reference for design.
5	VBATT_PWR	See JT2 pin 1
6	VBATT_PWR	See JT2 pin 1
7	VBATT_PWR	See JT2 pin 1
8	VBATT_PWR	See JT2 pin 1
9	VBATT_PWR	See JT2 pin 1
10	VBATT_PWR	See JT2 pin 1

Pin #	JT2 Signal Name	Description
11	VBATT_PWR	See JT2 pin 1
12	VBATT_PWR	See JT2 pin 1
13	VBATT_PWR	See JT2 pin 1
14	VBATT_PWR	See JT2 pin 1
15	VBATT_PWR	See JT2 pin 1
16	CS_PLUS	Current Sense (+) Terminal Sense
17	VBATT_PWR	See JT2 pin 1
18	CS_MINUS	Current Sense (-) Terminal Sense
19	VBATT_PWR	See JT2 pin 1
20	BATT_ID	Battery identification input to the PMI8998 PMIC on the SOM
21	VBATT_PWR	See JT2 pin 1
22	BATT_MINUS	Battery (-) Terminal Sense
23	VBATT_PWR	See JT2 pin 1
24	BATT_PLUS	Battery (+) Terminal Sense
25	USB_VBUS	PMI8998 USB charger input source. Output during OTG operation
26	HAP_OUT_N	Differential Haptics Drive Output.
27	USB_VBUS	See JT2 pin 25
28	HAP_OUT_P	Differential Haptics Drive Output.
29	USB_VBUS	See JT2 pin 25
30	VREG_L28A_3P0	LDO linear regulator L28 Default voltage = 3.00V Maximum Current = 150mA
31	USB_VBUS	See JT2 pin 25
32	BTN_PHONE_ON_N (KPD_PWR_N)	Power on input. Internally pulled up to +1.8V on SOM. Active low.
33	USB_VBUS	See JT2 pin 25
34	CAM2_STANDBY_N	CPU GPIO8
35	CBL_PWR_N	Cable Power Detect
36	BLSP8_UART_TX	CPU GPIO4. CPU Debug UART port
37	USB_CC2	USB Type-C Configuration Channels
38	BLSP8_UART_RX	CPU GPIO5. CPU Debug UART port
39	BL1_EN	PMI8998 GPIO14
40	ACCEL_INT	CPU GPIO117
41	CAM_IRQ	CPU GPIO24
42	BLSP9_SPI_CS_N	CPU GPIO51
43	CAM1_STANDBY_N	CPU GPIO27
44	BLSP9_SPI_CLK	CPU GPIO52
45	BAT_THERM	Battery thermistor input to the PMI8998 PMIC on the SOM



Pin #	JT2 Signal Name	Description
46	BLSP9_SPI_MISO	CPU GPIO50
47	WDOG_DISABLE (BOOT_CONFIG_0) (APQ_GPIO_101)	Boot configuration 0. Disables WatchDog timer.
48	BLSP9_SPI_MOSI	CPU GPIO49
49	HAP_CNTRL_ANLG	Haptic PWM control input.
50	LCD0_RESET_N	CPU GPIO94
51	MEMS_RESET_N	CPU GPIO80
52	FLASH_STROBE_EN	CPU GPIO21
53	USB_CC1	USB Type-C Configuration Channels
54	MDP_VSYNC_P	CPU GPIO10
55	HDMI_HOT_PLUG_DETECT	CPU GPIO34
56	MDP_VSYNC_S	CPU GPIO11
57	SD_CARD_DET_N	SD card detect signal. Pull high to VREG_S4A_1P8 with 100K resistor on carrier board
58	BLSP12_UART_TX	CPU GPIO81
59	HDMI_CEC	CPU GPIO31
60	BLSP12_I2C_SCL	CPU GPIO84.
61	HDMI_DDC_CLOCK	CPU GPIO32
62	BLSP12_I2C_SDA	CPU GPIO83.
63	BTN_RESIN_N (RESIN_N)	Reset input/Volume down. Internally pulled up to +1.8V on SOM. Active low
64	BLSP12_UART_RX	CPU GPIO82
65	FLASH_STROBE_TRIG	CPU GPIO22
66	HDMI_DDC_DATA	CPU GPIO33
67	BL0_EN	CPU GPIO135
68	APQ_GPIO132	Secure boot
69	GND	Ground reference for design.
70	GND	Ground reference for design.
71	MIPI_DSI0_LANE2_P	MIPI DSI data lane2 differential pair
72	MIPI_DSI0_LANE1_P	MIPI DSI data lane1 differential pair
73	MIPI_DSI0_LANE2_N	MIPI DSI data lane2 differential pair
74	MIPI_DSI0_LANE1_N	MIPI DSI data lane1 differential pair
75	GND	Ground reference for design.
76	GND	Ground reference for design.
77	MIPI_DSI0_LANE0_N	MIPI DSI data lane0 differential pair
78	MIPI_DSI1_LANE1_N	MIPI DSI data lane1 differential pair
79	MIPI_DSI0_LANE0_P	MIPI DSI data lane0 differential pair
80	MIPI_DSI1_LANE1_P	MIPI DSI data lane1 differential pair
81	GND	Ground reference for design.
82	GND	Ground reference for design.

Pin #	JT2 Signal Name	Description
83	MIPI_DSI0_CLK_N	MIPI DSI clock differential pair
84	MIPI_DSI1_LANE0_P	MIPI DSI data lane0 differential pair
85	MIPI_DSI0_CLK_P	MIPI DSI clock differential pair
86	MIPI_DSI1_LANE0_N	MIPI DSI data lane0 differential pair
87	GND	Ground reference for design.
88	GND	Ground reference for design.
89	MIPI_DSI1_CLK_P	MIPI DSI clock differential pair
90	MIPI_DSI1_LANE3_P	MIPI DSI data lane3 differential pair
91	MIPI_DSI1_CLK_N	MIPI DSI clock differential pair
92	MIPI_DSI1_LANE3_N	MIPI DSI data lane3 differential pair
93	GND	Ground reference for design.
94	GND	Ground reference for design.
95	MIPI_DSI0_LANE3_P	MIPI DSI data lane3 differential pair
96	MIPI_DSI1_LANE2_P	MIPI DSI data lane2 differential pair
97	MIPI_DSI0_LANE3_N	MIPI DSI data lane3 differential pair
98	MIPI_DSI1_LANE2_N	MIPI DSI data lane2 differential pair
99	GND	Ground reference for design.
100	GND	Ground reference for design.

Table 4 – B2B Connector JT3 Pin-outs

Pin #	JT3 Signal Name	Description
1	FAST_BOOT_2 (BOOT_CONFIG_3) (APQ_GPIO_104)	Boot configuration 3 (fast_boot_select bit 2). Configures external boot device.
2	VREG_L19A_3P0	LDO linear regulator L19 Default voltage = 3.00V Maximum Current = 600mA
3	APQ_GPIO42	CPU GPIO42
4	VREG_L19A_3P0	See JT3 pin 2
5	SDC2_CLK	SDC2 clock signal. Optional to pulled high to VREG_L13_2P95 on carrier board (not required)
6	VREG_L15A_1P8	LDO voltage switch L15 Default voltage = 1.80V Maximum Current = 300mA
7	SDC2_DATA3	SDC2, data bit 3. Optional to pulled high to VREG_L13_2P95 on carrier board (not required)
8	GND	Ground reference for design.
9	SDC2_DATA2	SDC2, data bit 2. Optional to pulled high to VREG_L13_2P95 on carrier board (not required)
10	NC	Not connected

Pin #	JT3 Signal Name	Description
11	SDC2_CMD	SDC2 CMD signal. Optional to pulled high to VREG_L13_2P95 on carrier board (not required)
12	NC	Not connected
13	SDC2_DATA1	SDC2, data bit 1. Optional to pulled high to VREG_L13_2P95 on carrier board (not required)
14	GND	Ground reference for design.
15	SDC2_DATA0	SDC2, data bit 0. Optional to pulled high to VREG_L13_2P95 on carrier board (not required)
16	USB3_HS_P	USB high-speed port differential pair
17	VREG_L16A_2P7	LDO voltage switch L16 Default voltage = 2.70V Maximum Current = 300mA
18	USB3_HS_N	USB high-speed port differential pair
19	VREG_L21A_2P95	LDO linear regulator L21 Default voltage = 2.95V Maximum Current (2pins) = 600mA
20	GND	Ground reference for design.
21	VREG_L21A_2P95	See JT3 pin 19
22	PM_VCOIN	Optional +3V coin cell backup battery connection to the PM8998 PMIC.
23	VREG_L13A_2P95	LDO linear regulator L13 Default voltage = 2.95V Maximum Current = 150mA
24	PCIE_WAKE	CPU GPIO37
25	MAG_DRDY_INT	CPU GPIO119
26	PCIE_RST_N	CPU GPIO35
27	CAM2_RST_N	CPU GPIO9
28	CAM0_STANDBY_N	CPU GPIO29
29	TS0_RESET_N	CPU GPIO89
30	PCIE1_CLKREQ_N	CPU GPIO36
31	APQ_GPIO149	CPU GPIO149
32	TS_INT0	CPU GPIO125
33	CAP_INT_N	CPU GPIO123
34	BLSP6_I2C_SDA	CPU GPIO43. Pulled up to VREG_S4A_1P8 via 1K resistor on dev kit carrier for PCIe.
35	BLSP1_SPI_CS_N	CPU GPIO2
36	VREG_L14A_1P8	LDO linear regulator L14 Default voltage = 1.80V Maximum Current = 300mA
37	BLSP1_SPI_MOSI	CPU GPIO0

Pin #	JT3 Signal Name	Description
38	BLSP6_I2C_SCL	CPU GPIO44. Pulled up to VREG_S4A_1P8 via 1K resistor on dev kit carrier for PCIe.
39	BLSP1_SPI_MISO	CPU GPIO1
40	CODEC_RESET_N	Reset Signal to Codec (Active Low) CPU GPIO64
41	BLSP1_SPI_CLK	CPU GPIO3
42	CAM0_RST_N	CPU GPIO30
43	GYRO_INT	CPU GPIO118
44	APQ_GPIO41	CPU GPIO41
45	GND	Ground reference for design.
46	SBU_SW_OE (SBU1)	USB Type-C SBU (1 of 2) switch isolation and reversibility control
47	CODEC_INT1_N	Interrupt #1 from Codec (Active Low) CPU GPIO54
48	MI2S_1_SCK	MI2S Interface #1, bit clock CPU GPIO65
49	CDC_MCLK	PM8998 GPIO13
50	MI2S_1_WS	MI2S Interface #1, word select CPU GPIO66
51	VREG_L24A_3P075	LDO linear regulator L24 Default voltage = 3.075V Maximum Current = 150mA
52	MI2S_1_Do	MI2S Interface #1, serial data channel 0 CPU GPIO67
53	GND	Ground reference for design.
54	SLIMBUS_DATA0	SLIMbus Audio Interface, data bit 0 CPU GPIO71
55	LNBB_CLK2	Low Noise Baseband clock 2
56	SLIMBUS_CLK	SLIMbus Audio Interface, clock CPU GPIO70
57	APQ_GPIO96	CPU GPIO96
58	SLIMBUS_DATA1	SLIMbus Audio Interface, data bit 1 CPU GPIO72
59	GND	Ground reference for design.
60	SSC_PWR_EN	CPU SSC1
61	APQ_RESOUT_N	CPU reset output
62	SSC_SPI_1_CLK	CPU SSC9
63	SBU_SW_SEL (SBU2)	USB Type-C SBU (2 of 2) switch isolation and reversibility control
64	SSC_SPI_1_CS_N	CPU SSC8
65	ALSPG_INT_N	CPU GPIO120
66	SSC_SPI_1_MOSI	CPU SSC10
67	QNOVO_EXT_FET_CTL	PMI8998 GPIO6
68	SSC_SPI_1_MISO	CPU SSC11

Pin #	JT3 Signal Name	Description
69	HRM_INT	CPU GPIO122
70	SSC_SPI_1_CS1_MAG_N	CPU SSC0
71	VREG_S4A_1P8	Switched-mode power supply S4 Default voltage = 1.80V Maximum Current (2pins) = 600mA <sup>1</sup>
72	SSC_UART_2_RX	CPU SSC15
73	VREG_S4A_1P8	See JT3 pin 71
74	SSC_I2C_3_SCL	CPU SSC3
75	PMI_CHARGE_STAT	PMIC charging status signal
76	SSC_UART_2_TX	CPU SSC14
77	RED_LED_DRV	PMI8998 RGB PWM LED output
78	SSC_I2C_3_SDA	CPU SSC2
79	GREEN_LED_DRV	PMI8998 RGB PWM LED output
80	QUA_MI2S_DATA3	MI2S Interface #4, serial data channel 3 CPU GPIO63
81	BLUE_LED_DRV	PMI8998 RGB PWM LED output
82	QUA_MI2S_DATA0	MI2S Interface #4, serial data channel 0 CPU GPIO60
83	VREG_WLED	White LED boost SMPS source
84	QUA_MI2S_DATA1	MI2S Interface #4, serial data channel 1 CPU GPIO61
85	WLED_SINK1	White LED low-side current sink input
86	QUA_MI2S_WS	MI2S Interface #4, word select CPU GPIO59
87	WLED_SINK3	White LED low-side current sink input
88	QUA_MI2S_SCK	MI2S Interface #4, bit clock CPU GPIO58
89	WLED_SINK2	White LED low-side current sink input
90	QUA_MI2S_DATA2	MI2S Interface #4, serial data channel 2 CPU GPIO62
91	VREG_DISP	SMPS output, display positive bias. Default voltage = 5V5
92	CAM1_RST_N	CPU GPIO28
93	CABC	PWM input for dynamic dimming
94	FAST_BOOT_0 (BOOT_CONFIG_1) (APQ_GPIO_102)	Boot configuration 1 (fast_boot_select bit 0). Configures external boot device
95	VREG_DISN	SMPS output, display negative bias. Default voltage = -5V5
96	TYPEC_UUSB_SEL	microUSB or USB Type-C connector type select
97	LCD_AMOLED_SEL	PMI8998 GPIO7
98	FAST_BOOT_1 (BOOT_CONFIG_2) (APQ_GPIO_103)	Boot configuration 2 (fast_boot_select bit 1). Configures external boot device.

Pin #	JT3 Signal Name	Description
99	CODEC_INT2_N	Interrupt #2 from Codec (Active Low) CPU GPIO53
100	FORCED_USB_BOOT (APQ_GPIO_57)	Forced USB boot

NOTE 1: The VREG\_S4A\_1P8 power rail is also used by circuits on the SOM.

### 4.3 RF Antenna Connections

The Open-Q 835  $\mu$ SOM provides WIFI and Bluetooth connectivity via the Qualcomm WCN3990 chipset. This provides 802.11a/b/g/n/ac 2x2 MIMO, dual-band Wi-Fi, and Bluetooth 5.x. The 2x2 MIMO Wi-Fi requires two antennas for maximum throughput and operates at both 2.4GHz and 5GHz. Bluetooth uses only one of the antennas (CH0) and only operates at 2.4GHz. To support full performance of the Wi-Fi and Bluetooth, two dual-band antennas are required. If only Bluetooth is used, it can be supported with one single-band 2.4GHz antenna connected to the CH0 port.

The SOM uses two U.FL coaxial connectors (Hirose U.FL-R-SMT-1 (10)) for the antenna ports, as shown in the Figure 2 above.

**Table 5 – RF Signals via U.FL Coaxial Receptacles**

Antenna	Description	Notes
Antenna CH0	RF chain 0 interface to Qualcomm WCN3990 chipset for Wi-Fi/BT	Antenna port for Wi-Fi and Bluetooth
Antenna CH1	RF chain 1 interface to Qualcomm WCN3990 chipset for Wi-Fi	Second antenna port for Wi-Fi 2x2 MIMO

The Open-Q 835  $\mu$ SOM has received certification with FCC and Industry Canada as a modular radio transmitter for WLAN and Bluetooth. These certifications apply so long as the antenna structures and transmit powers used are equivalent to those used for the original certification. Changes to firmware, drivers, or board configuration files may have an impact to transmit power. For this reason, it is recommended to refer to the SOM certification documents (see document R-4) and section 9.1 below for information regarding the test configurations used for certification. Deviating from the documented configuration may trigger the need for re-certification.

## 5. ELECTRICAL SPECIFICATIONS

The input power to the SOM is provided by a power supply (battery or wall adapter) and also a USB source, for battery charging purposes. All input power sources enter the PMI8998 power management IC on the SOM, which then distributes power (along with the PM8998 and PM8005 PMICs) to other circuits on the SOM and connected carrier board via LDO and switching power supply outputs.

### 5.1 Absolute Maximum Ratings

The table below shows the absolute maximum ratings in which the SOM input power sources can be exposed to without experiencing functional failure.

**Table 6 – Absolute Maximum Input Power Ratings**

Parameter	Min	Max	Units
Battery or DC power input (SOM_SYS_PWR)	-0.3	6	V
USB VBUS battery charger input voltage source (USB_VBUS)	-0.3	28	V

### 5.2 Operating Conditions

The table below shows the recommended operating conditions for the SOM to meet all performance specifications (provided the absolute maximum ratings have never been exceeded).

**Table 7 – Operating Input Power Ratings**

Parameter	Min	Typ	Max	Units
Battery or DC power input (SOM_SYS_PWR)	3.45 <sup>1</sup>	3.8	4.2	V
USB VBUS battery charger input voltage source (USB_VBUS)	3.6	5	14	V
PM_VCOIN Input		3.2		V

### 5.3 Operating Temperature

The SOM operating temperature ratings listed below are based only on the component case temperature ratings of individual components populated on the SOM. Users should consider the specific environmental conditions in which the final product is used in.

**Table 8 – Operating temperature range (Tc)**

Parameter	Min	Typ	Max	Units
Overall SOM (case temperature)	-25	+25	+85	°C

<sup>1</sup> The SOM may be configured to operate at lower input voltage levels but changes to bootloader or proprietary code are needed and this will require support from Intrinsic. Intrinsic's solutions and software engineering services can provide advice and support for specialty low voltage requirements. Please contact Intrinsic sales at: <https://www.intrinsic.com/sales-inquiry>

## 5.4 Power Consumption

Power consumption measurements have been performed on the SOM running Android 8.0 under common operational modes. All tests were executed at room temperature and with the default thermal solution that ships with the SOM development kit (heat sink on top of CPU) unless noted otherwise. In some test cases, ADB was used to monitor the SOM to ensure that the CPU was not throttling during the test. If ADB is not used, power consumption may be lower.

The table below contains the SOM power consumption numbers under common operational modes.

**Table 9 – Power Consumption Ratings**

Operational Modes	Description	Average	Peak
Boot	Power consumption during boot process	n/a	5.47W
Suspend (Wi-Fi Off)	SOM placed in standby (Wi-Fi Off, Display Off)	27.7mW	30.3mW
Suspend (Wi-Fi On)	SOM placed in standby (Wi-Fi On, Display Off)	130mW	1.59W
Idle (Wi-Fi Off)	SOM is idle (Wi-Fi Off, Display On)	260mW	1.12W
Idle (Wi-Fi on)	SOM is idle (Wi-Fi On, Display On)	301mW	1.36W
Video Record (1080P)	SOM recording 1080P video	913mW	2.05W
Video Record (4K UHD)	SOM recording 4K UHD video	1.49W	2.90W
Video Playback (1080P)	SOM playing back 1080P video	468mW	1.76W
Video Playback (4K UHD)	SOM playing back 4K UHD video	598mW	2.31W
Audio Playback	SOM playing back MP3 (Display Off)	109mW	953mW
Wi-Fi Download	SOM downloading data over Wi-Fi (Display Off)	804mW	2.04W
Wi-Fi Upload	SOM uploading data over Wi-Fi (Display Off)	2.05W	2.78W
Full Load (Quad Core)	Running all 4 cores	4.55W	5.24W
Full Load (Single Core)	Running only cpu0	911mW	1.03W
UFS Write	Writing data to UFS (Display Off)	1.32W	1.92W
UFS Read	Reading data from UFS (Display Off)	1.26W	1.38W
Bluetooth	SOM playing music over Bluetooth (Display Off)	134mW	1.03W

### NOTES:

- The full load (Quad Core) test used a fan pointed at the heatsink to prevent thermal throttling of the CPU.

## 5.5 ESD Ratings

The SOM is not designed with additional ESD protection other than what is included in the integrated circuits. It is recommended to take proper precautions in a static free environment when handling the SOM.

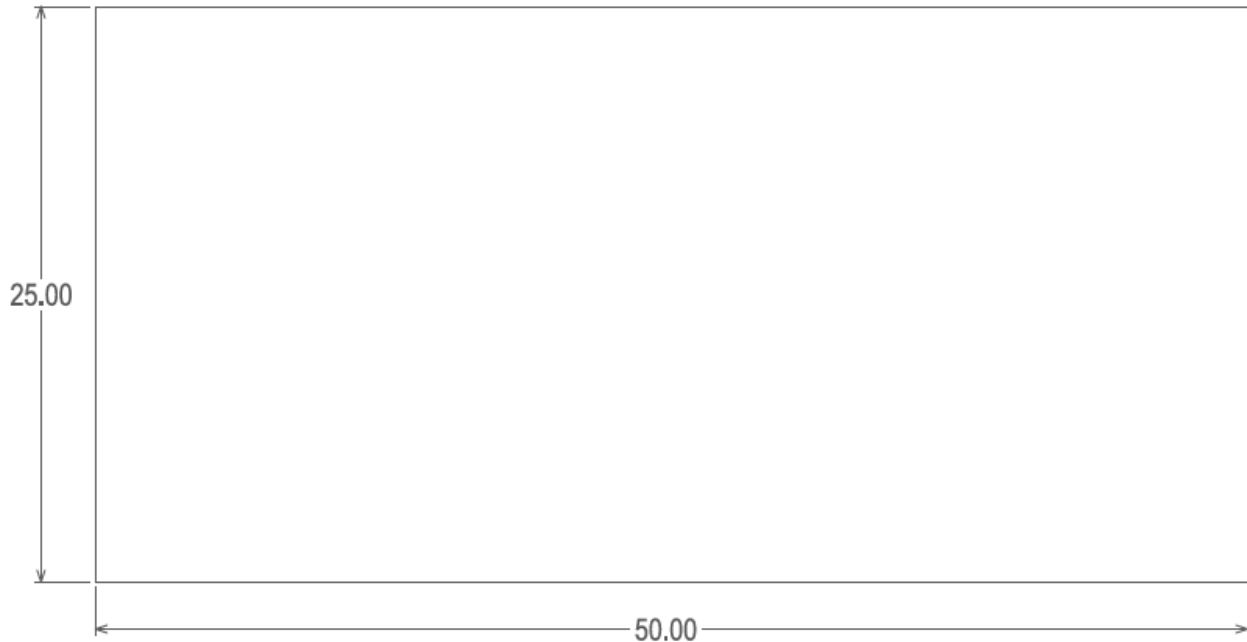


## 6. MECHANICAL SPECIFICATIONS

The sections below present some mechanical details of the Open-Q 835  $\mu$ SOM. For access to the 3D design files, please see <http://tech.intrinsyc.com/> (dev kit registration required).

### 6.1 SOM Mechanical Outline

The outer dimensions of the SOM are 50.0 x 25.0mm, as shown below. The key inner-dimensions for the SOM relate to connector positioning; these dimensions are called out later in this document.



**Figure 5 - SOM Mechanical Outline**

### 6.2 Top and Bottom Height Restrictions

The tallest component on the top-side of the SOM is 1.46mm (WIFI/BT Shield). Please note that when the mating coax cables are connected, the top side height may be higher.

The tallest component, other than the board to board connectors, on the bottom-side of the SOM is 1.0mm (inductors L18-L22).

NOTE: When designing the Carrier Board PCB, components should not be placed in the area immediately underneath the SOM.

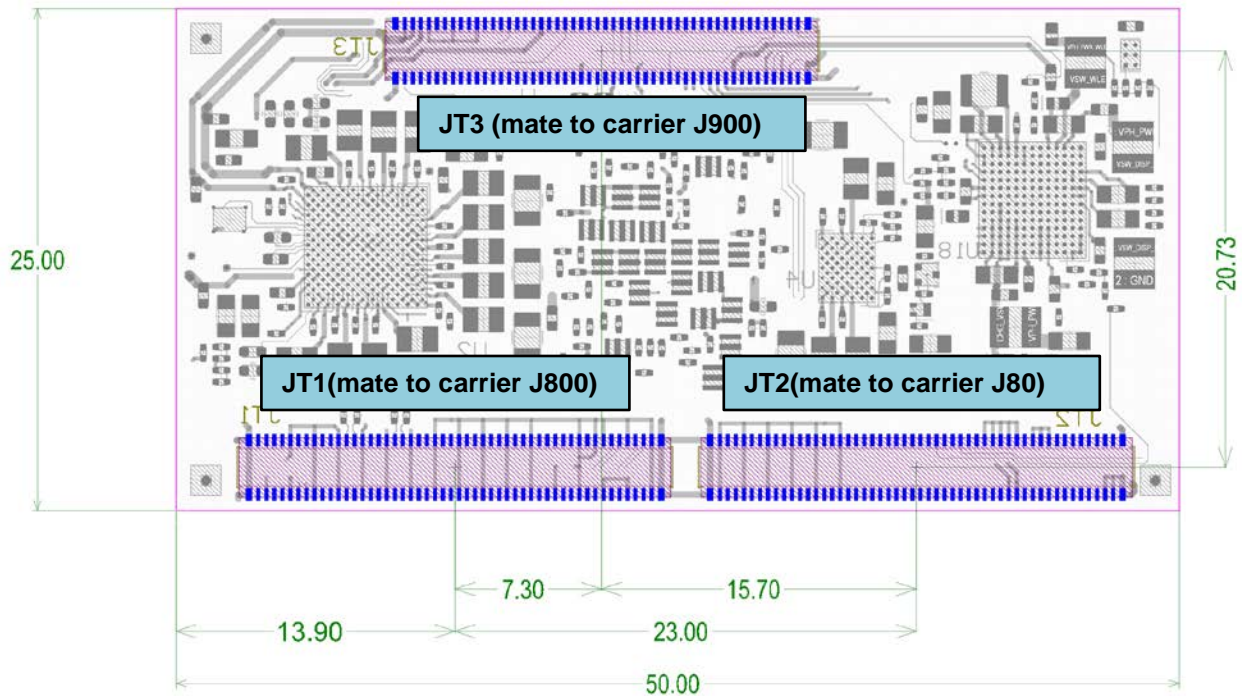
### 6.3 Landing Pattern

Dimensions presented are in millimeters (mm). The footprint information in this section can be used as a guide when designing a landing area for the SOM.

Dimensions show the relative position of each connector on the SOM; referenced to the center of the connector body. NOTE: This information is given for reference. It is highly recommended

that the Open-Q 835  $\mu$ SOM Carrier Board design source files and document R-2 be used to ensure proper dimensioning on any custom carrier board design.

\*The perspective of this figure is looking through the top side of the SOM.



**Figure 6 - SOM Land-Pattern Dimensions (mm)**

The mating connector, Hirose DF40X-X-100DS-0.4V, is available in different heights, to achieve stack heights of 1.5mm or 3.0mm.

## 6.4 Thermal Characteristics

The APQ8098 has built in thermal protections which will reduce processor frequency as the die temperature approaches set operating limits. These limits protect the processor from damage that could be caused by elevated die temperature. Additional product-level thermal management will remove heat from the SOM and its components, allowing the processor to run at higher frequencies for longer time periods before approaching the built in die temperature limits. This enables the average processor speed to remain higher through processor-intensive applications. Effectively removing heat from the Open-Q 835  $\mu$ SOM is required to optimize system performance and efficiency and to ensure that the APQ8098 processor can perform as desired.

For more information on thermal mitigation, see SOM Carrier Board Design Guide (Reference document R-2).

## 6.5 Weight

The SOM weighs approximately 16 grams.

## 7. PRODUCT MARKING, ORDERING, AND SHIPPING INFO

### 7.1 Product Marking

The SOM part number and product marking can be identified on the white label on the top of the module. The figure and table below show a label example which includes the SOM name and QR code.



Figure 7 – Open-Q 835  $\mu$ SOM Label (top of PCB)

Table 10 –Open-Q 835  $\mu$ SOM Label Marking

Line	Marking	Description/ Notes
1	Open-Q 835 $\mu$ SOM	Intrinsyc Technologies product name
2	QR code *	<p>Embeds serial number and Wi-Fi MAC address. The serial number format is VVV-WWXX-YYYYYY-ZZZZZ</p> <ul style="list-style-type: none"> <li>- VVV = Product number</li> <li>- WW = PCB revision number</li> <li>- XX = BOM revision number</li> <li>- YYYYYY = Date of manufacture (mm/dd/yy)</li> <li>- ZZZZZ = Unique serial number for PCB</li> </ul> <p>The MAC address format is 0123456789AB</p> <ul style="list-style-type: none"> <li>- 12 hexadecimal digit MAC address</li> </ul>
<p>* QR code reader mobile app (e.g. Neo Reader) can be used to read embedded serial number and the MAC address.</p>		

## 7.2 Product Ordering Information

When available, the Open-Q 835  $\mu$ SOM can be ordered for evaluation and prototype use from the Intrinsic online store at <http://shop.intrinsic.com>. For volume production orders or for custom requirements please contact Intrinsic sales at <https://www.intrinsic.com/sales-inquiry>.

Orderable Part Numbers	
Open-Q 835 $\mu$ SOM	QC-DB-L10004
Open-Q 835 $\mu$ SOM Development Kit	QC-DB-L10003

## 7.3 Packaging and Shipping Information

The Open-Q 835  $\mu$ SOM is packaged individually in small anti-static bags and bubble-wrap bags for protection during shipping – see Figure 9 below. They are then put into different sized boxes depending upon the quantity of the order. Small quantities are shipped in standard courier boxes with bubble-wrap protection and large quantity orders are packaged in a carton with dividers, as shown in Figure 10, below.



Figure 8 - Individual SOM Packaging



Figure 9 - Packaging for Large Quantity Shipments

## 8. HANDLING PRECAUTIONS

### 8.1 ESD Precautions

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

The Open-Q 835  $\mu$ SOM is designed as a component meant to be integrated into a final product and therefore has no additional ESD protection built-in. It should be handled only in a static-safe environment to prevent damage.

### 8.2 SOM – Carrier Board Mating Cautions

Caution must be taken when connecting or disconnecting the SOM to a carrier board to prevent damage. Ensure that the SOM is inserted and removed straight up and down to prevent any sideways force on the connectors which could damage them.

Also note that the DF40C-100DX board to board connectors are rated for a maximum of 30 mating / un-mating cycles. Therefore the number of insertions and removals must be limited to ensure reliability of the connectors.

### 8.3 Storage

The SOM must be stored in an antistatic bag.

## 9. CERTIFICATION

### 9.1 Radio Certification

The Intrinsic Open-Q 835  $\mu$ SOM has been certified with FCC and Industry Canada as a modular radio transmitter for WLAN and Bluetooth. The FCC and Industry Canada ID numbers are:

- FCC ID: 2AFDI-ITCOQ835S
- IC: 9049A-ITCO835S

These certifications apply so long as the antenna structures and transmit powers used are equivalent to those used for the original certification. Changes to firmware, drivers, or board configuration files may have an impact to transmit power. For this reason, it is recommended to refer to the SOM certification documents (see document R-4) for information regarding the test configurations used for certification. Deviating from the documented configuration may trigger the need for re-certification.

### 9.2 ROHS/REACH Compliance

The Intrinsic Open-Q 835  $\mu$ SOM complies with the ROHS/REACH standard. The certificate of compliance is available at <http://tech.intrinsic.com> (dev kit registration required).

## 10. COMPANY CONTACT

For more information, support or sales, please contact us.

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