Open-Q 835 µSOM Development Kit

User Guide

[Document: ITC-01RND1265-UG-001 Version: 1.0]

IDENTIFICATION

Document Title	Open-Q 835 µSOM Development Kit User Guide
Document Number	ITC-01RND1265-UG-001
Version	1.0
Date	Jan 18, 2019

Revision History

REVISION	DATE	DESCRIPTION	PAGES
1.0	Jan 18, 2019	First Release	All

Table of Contents

1. INTRODUCTION

1.1 Purpose

The purpose of this user guide is to provide primary technical information on the Open-Q 835 µSOM Development Kit.

For more background information on this development kit, visit: www.intrinsyc.com

1.2 Scope

This document will cover the following items on the Open-Q 835 µSOM Development Kit:

- Block Diagram and Overview
- Hardware Features
- Configuration
- µSOM
- Carrier Board
- Display Board for LCD (Optional)

1.3 Intended Audience

This document is intended for users who would like to develop custom applications on the Intrinsyc Open-Q 835 µSOM Development Kit.

2. DOCUMENTS

This section lists the supplementary documents for the Open-Q 835 µSOM development kit.

2.1 Applicable Documents

REFERENCE	TITLE
A-1	Intrinsyc Purchase and Software License Agreement for the Open-Q Development Kit

2.2 Reference Documents

REFERENCE	TITLE
R-1	Open-Q 835 Schematics (µSOM, Carrier)
R-2	Open-Q 835 Dev Kit µSOM Tech Note 43, 835 SOM Carrier Board Design Guide

2.3 Terms and Acronyms

Term and acronyms	Definition
AMIC	Analog Microphone
ANC	Audio Noise Cancellation
B2B	Board to Board
BLSP	Bus access manager Low Speed Peripheral (Serial interfaces like UART / SPI / I2C/ UIM)
BT LE	Bluetooth Low Energy
CSI	Camera Serial Interface
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read only memory
eMMC	Embedded Multimedia Card
FCC	US Federal Communications Commission
FWVGA	Full Wide Video Graphics Array
GPS	Global Positioning system
HDMI	High Definition Media Interface
HSIC	High Speed Inter Connect Bus
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MIPI	Mobile Industry processor interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
RF	Radio Frequency
SATA	Serial ATA
SLIMBUS	Serial Low-power Inter-chip Media Bus
µSOM	micro System On Module

SPMI	System Power Management Interface (Qualcomm® PMIC / baseband proprietary protocol)
SSBI	Single wire serial bus interface (Qualcomm® proprietary mostly PMIC / Companion chip and baseband processor protocol)
UART	Universal Asynchronous Receiver Transmitter
UFS	Universal Flash Storage
UIM	User Identity module
USB	Universal Serial Bus
USB HS	USB High Speed
USB SS	USB Super Speed

2.4 List of Figures

2.5 List of Tables

3. OPEN-Q 835 µSOM DEVELOPMENT KIT

3.1 Introduction

The Open-Q 835 µSOM provides a quick reference or evaluation platform for Qualcomm's latest 835 series - Snapdragon 835 processor. This kit is suited for Android / Linux application developers, OEMs, consumer manufacturers, hardware component vendors, video surveillance, robotics, camera vendors, and flash chip vendors to evaluate, optimize, test and deploy applications that can utilize the Qualcomm® Snapdragon 835 series technology.

3.2 Development Platform Notice

This development platform contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development platform may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at http://www.fcc.gov/oet/rfsafety/

3.3 Handling Precautions

3.3.1 Handling

WARNING! The Open-Q 835 µSOM Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist or foot strap

3.3.2 Storage

The kit should always be stored inside an anti-static bag.

3.4 Kit Contents

The Open-Q 835 µSOM Development Kit includes the following:

- Open-Q 835 µSOM with the Snapdragon 835 (APQ8098) processor or main CPU board
- Mini-ITX form-factor carrier board
- 4.5” FWVGA (480x854) 16.7 M LCD (Additional Accessory)
- AC power adapter and HDMI cable

Figure 1 Assembled Open-Q 835 µSOM Development Kit

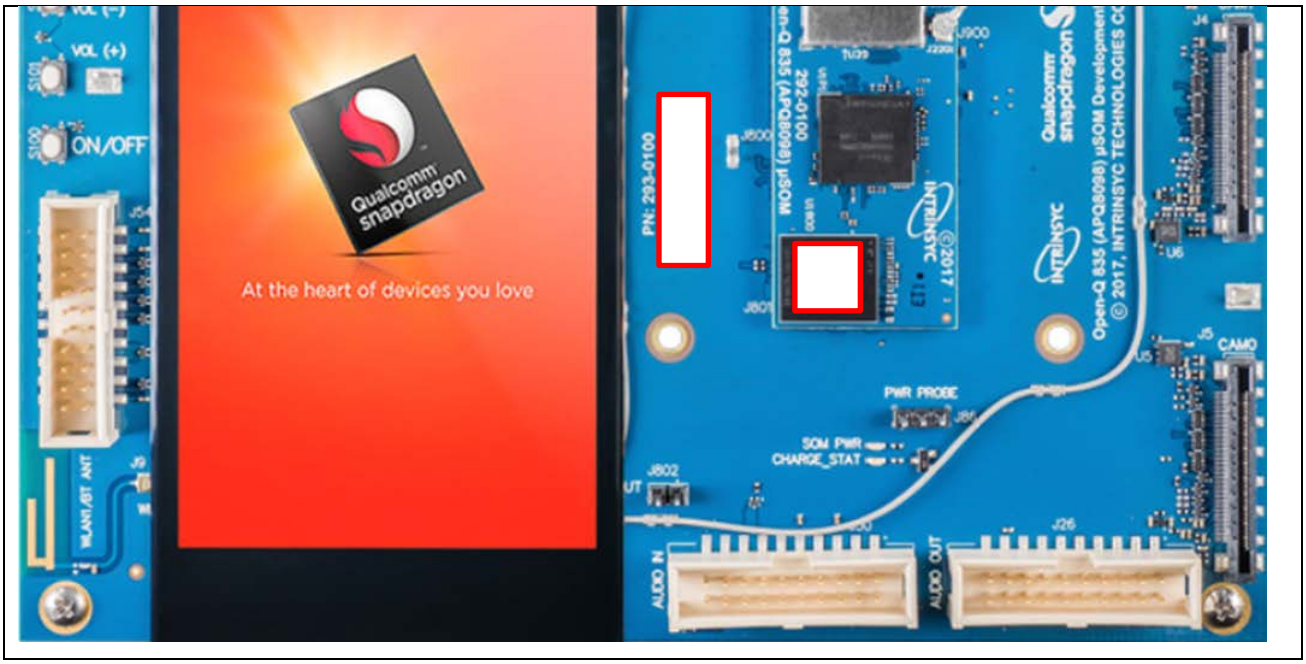
The development kit comes with Android software pre-programmed on the CPU board (µSOM). Please contact Intrinsyc for availability of camera modules, sensor boards, and other accessories: sales@intrinsyc.com

3.5 Hardware Identification Label

Labels are present on the CPU board and the mini-ITX form-factor carrier board. The following information is conveyed on these two boards:

CPU board (µSOM).:

- Serial Number
- WIFI MAC address



Refer to http://support.intrinsyc.com/account/serialnumber for more details about locating the serial number, as this will be needed to register the development kit. To register a development kit, please visit: http://support.intrinsyc.com/account/register

Mini-ITX form-factor carrier board:

- Serial Number

Note: Please retain the µSOM and carrier board serial number for warranty purposes.

3.6 Powering-Up the Development Kit the first time

WARNING! Before powering up the development kit the first time, please do complete reading this user guide.

3.7 System Block Diagram

The Open-Q 835 µSOM development platform consists of three major components

- Open-Q 835 µSOM
- Carrier board for I/O and connecting with external peripherals
- Display Adapter Board (additional accessory)

The following diagram explains the interconnectivity and peripherals on the development kit.

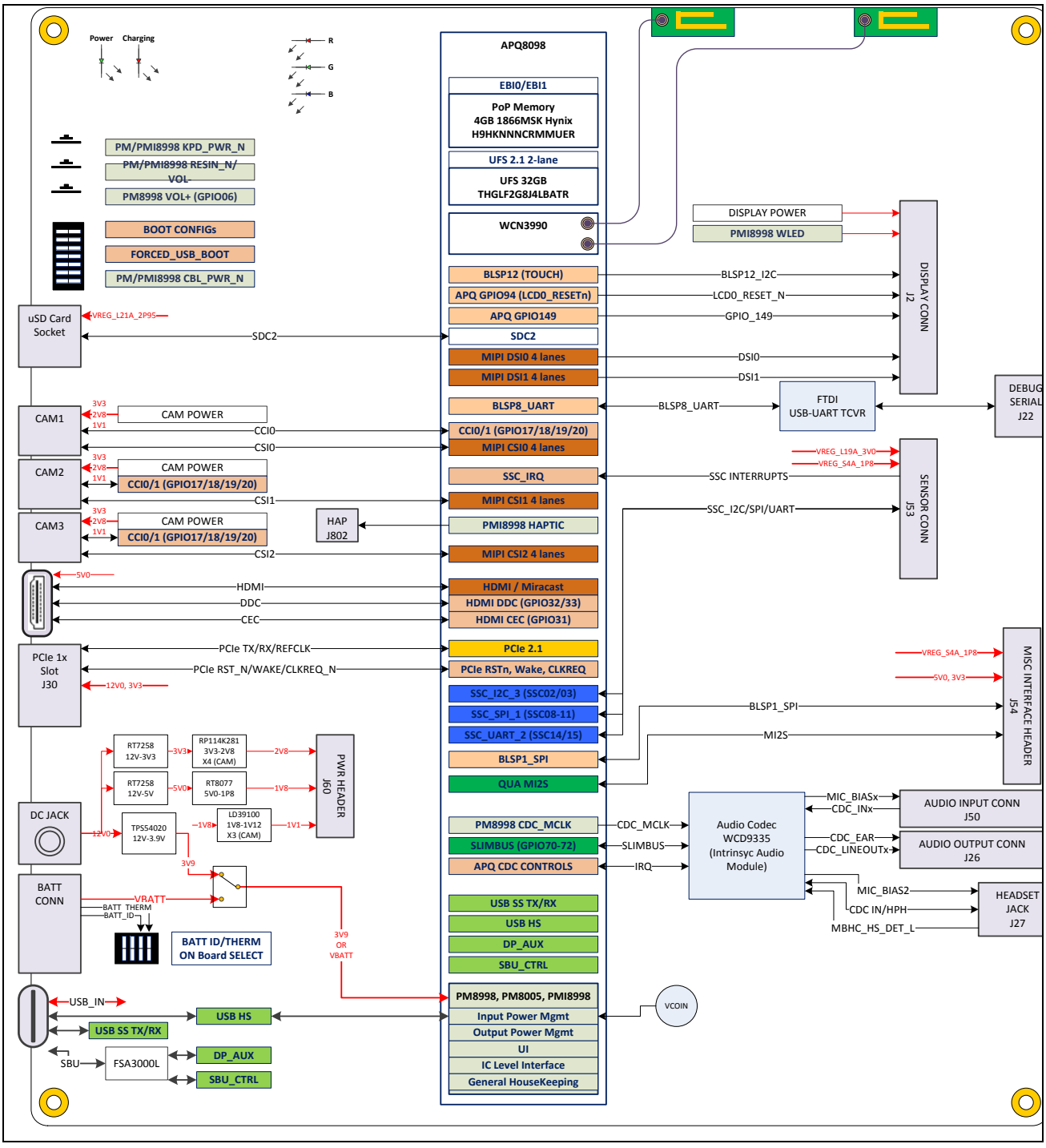


Figure 2 Open-Q 835 µSOM + Carrier Board Block Diagram

3.8 Open-Q 835 µSOM

The µSOM provides the basic common set of features with minimal integration efforts for end users.

It contains the following:

- Snapdragon 835 (APQ8098) main application processor
- LPDDR4 up to 1866MHz 4GB RAM (POP)
- PMI8998 + PM8998 + PM8005 – PMIC for Peripheral LDOs, Boost Regulators
- WCN3990 Wi-Fi + BT combo chip
- 32 GB UFS 2.0

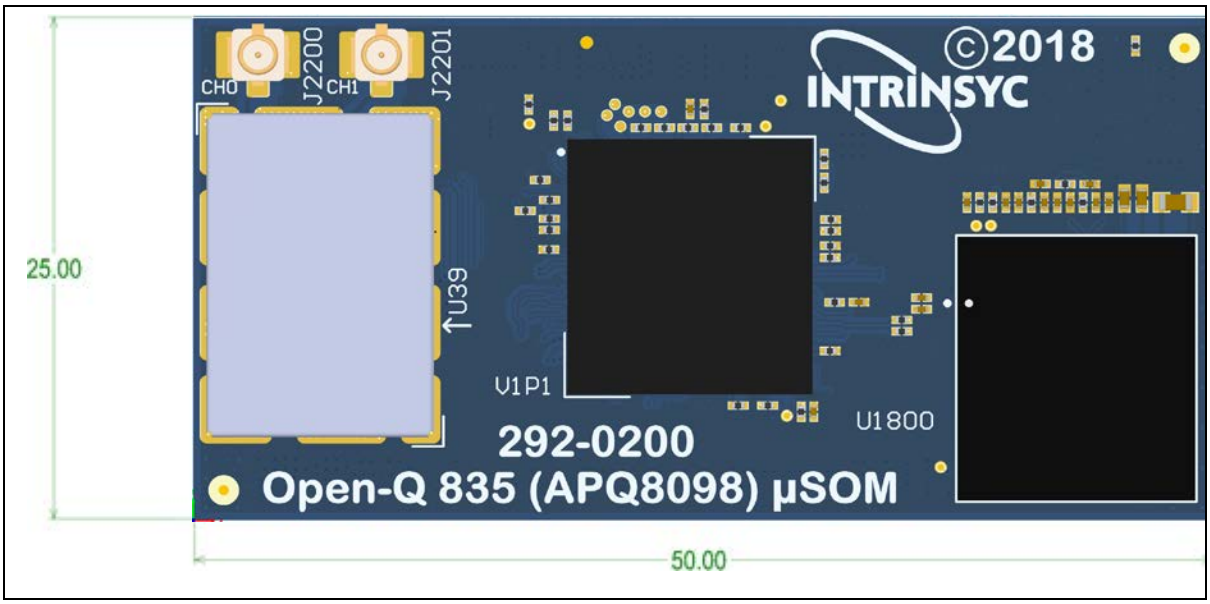


Figure 3 Open-Q 835 µSOM (Top View)

3.8.1 µSOM Mechanical Properties

Area	12.5 cm^2(25 mm x 50 mm)
Interface	3 x 100-pins Hirose DF40 connectors (B2B Connector).
Thermal	A top side heat sink is installed by default.
Shielding	A top side shield can for the WiFi/BT Circuitry is installed by default.

3.8.2 Hardware Specification

The Open-Q 835 µSOM platform encompasses the following hardware features:

Table 1 Open-Q 835 µSOM Hardware Features

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	APQ8098	Qualcomm® Snapdragon 835 Processor	Qualcomm® Kyro CPU, quad core, 64-bit ARM V8 compliant processor, 2.2GHz
	PMIC (PMI8998, PM8998, PM8005)	Qualcomm® PMIC, Companion PMIC for APQ8098 processor	NA
Memory	4GB LPDDR4	Memory POP	Up to 1866MHz LPDDR4 POP on CPU BGA chip. Supports via 4x16bit channels
	32 GB UFS	Primary Storage for platform. Mainly used for storing SW applications and user data etc.	Toshiba UFS on board. Can support up to 256GB
RF Connectivity	Wi-Fi 2.4 GHz/ 5GHz via WCN3990	Wi-Fi WCN3990 Wi-Fi + BT Combo Chip	802.11a/b/g/n/ac 2.4/5.0 GHz via WCN3990. Full 2x2 antenna configuration
	BT 2.4 GHz via WCN3990	Wi-Fi WCN3990 Wi-Fi + BT Combo Chip	Support Bluetooth 5 (LE 5.x + HS)
RF Connector	WLAN/BT Ant x 1 WLAN Ant x 1	Two U.FL connectors to connect to antennas on carrier board via coax cable	2.4/ 5 GHz
Multimedia	4-lane MIPI CSI x 3	Three Camera Interfaces CSI0, CSI1 and CSI2	MIPI CSI D-PHY v1.2
	4-lane MIPI DSI x 2	Two Display DSI interfaces DSI0 and DSI1	MIPI DSI D-PHY v1.2
	HDMI x 1	One HDMI video output interface	HDMI v2.0a
BaseBand Connectivity	USB x 1	One USB 3.1 which can Type-C with Display Port	USB3.1 & USB2.0
	PCIe x 1	One PCI-SIG PCIe interface	v2.1 PHY v2.1 controller
	SDIO x 1	4-bit port for SD/MMC card	SD3.0
	BLSP ports	Multiple BLSP ports are routed out and configurable for UART, I2C, SPI, or GPIO	
	Audio ports	Multiple Audio ports are routed out and configurable for SLIMBus, MI2S, PCM, or GPIO	
Connector	board to board connector x 3	Three connectors to interface with carrier board	Hirose DF40C series 100pin connector

3.8.3 µSOM RF Specification for WIFI and BT

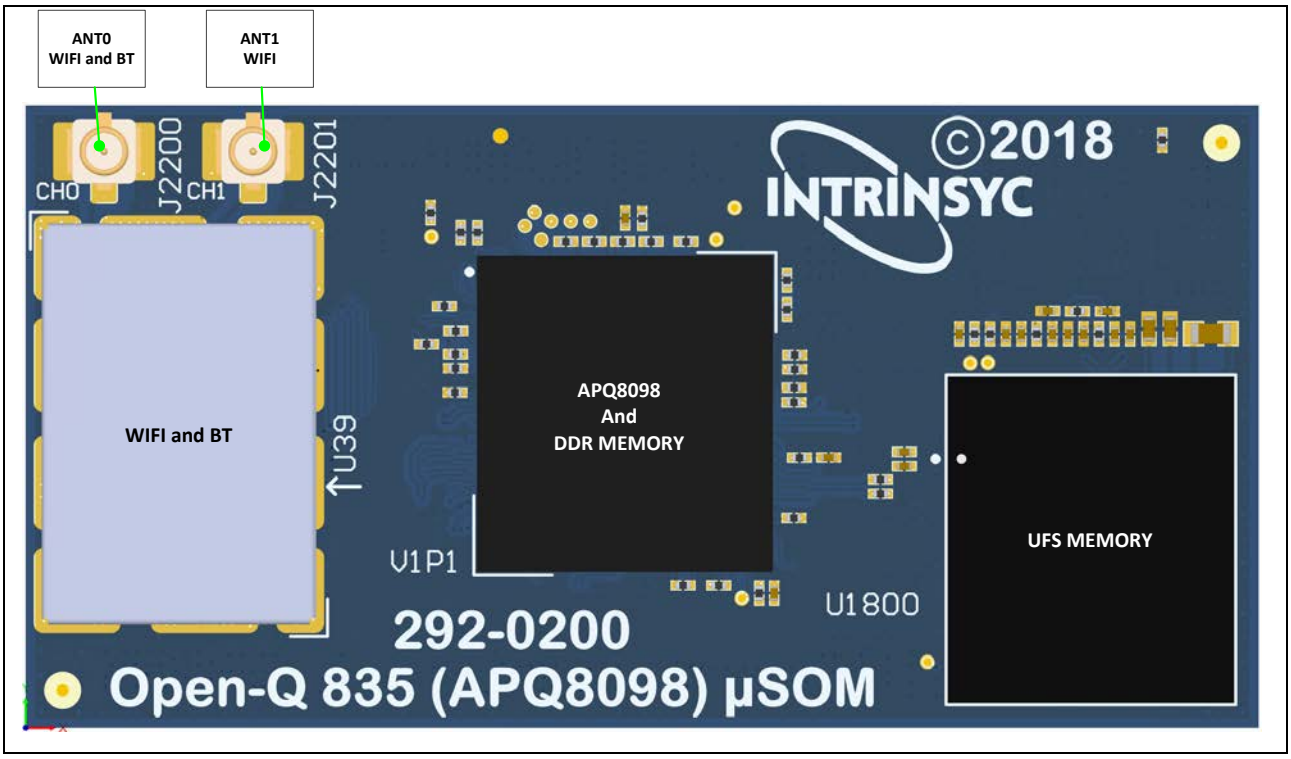


Figure 4 Open-Q 835 SOM (Top View)

The µSOM includes the following radio interfaces:

- Wi-Fi + BT: CH0 – ANT0
- Wi-Fi only: CH1 – ANT1

ANT0: Channel 0 is used for providing Wi-Fi and Bluetooth connectivity to WCN3990. This antenna connector is meant to be connected to the carrier board via a coaxial cable.

ANT1: Channel 1 provides Wi-Fi connectivity for WCN3990. This antenna connector is meant to be connected to the carrier board via a coaxial cable. This channel does not support Bluetooth connectivity.

3.9 Open-Q 835 µSOM Carrier Board

The Open-Q 835 µSOM Carrier board is a Mini-ITX form factor board with various connectors used for connecting different peripherals.

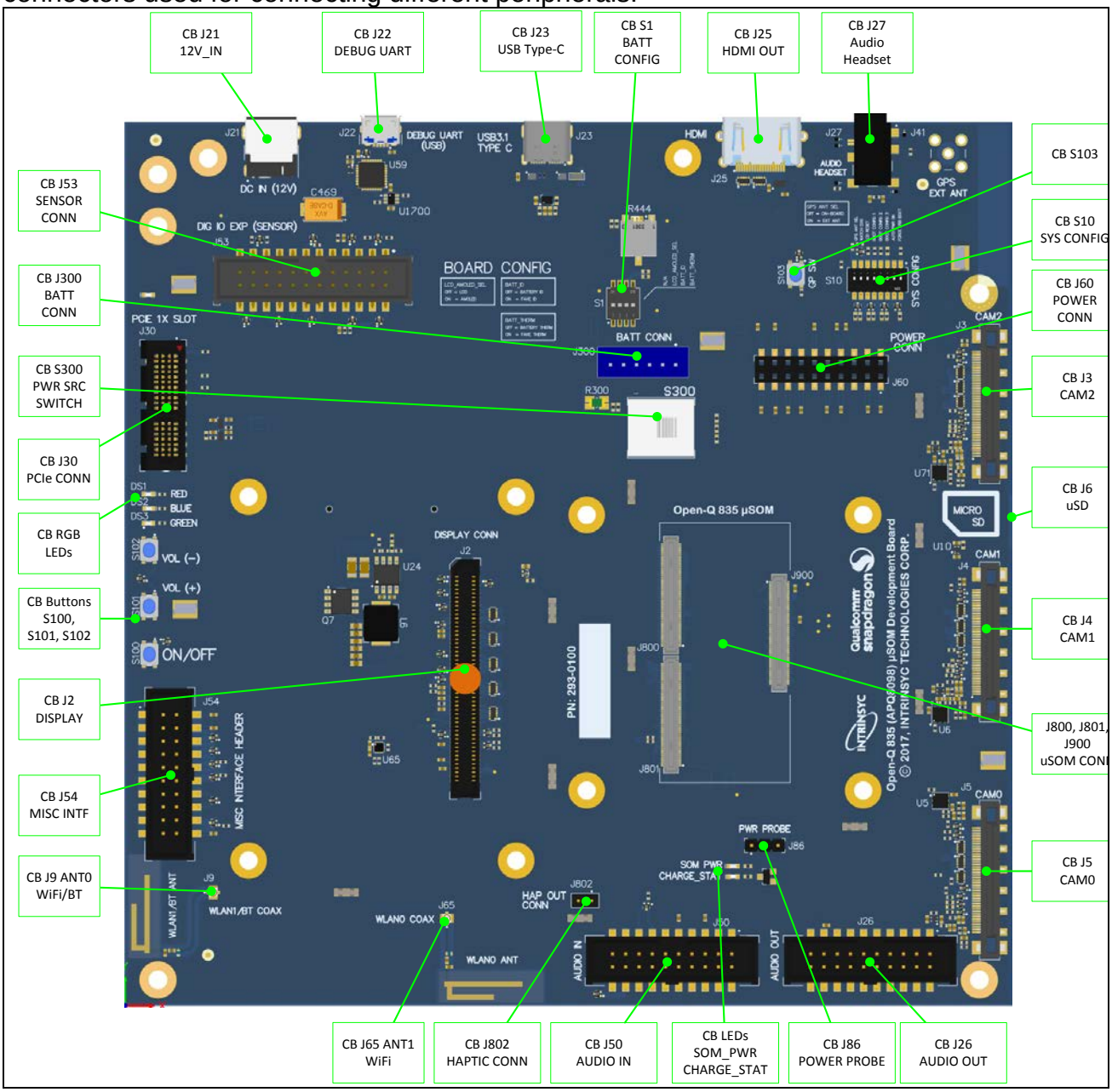


Figure 5 Open-Q 835 Carrier Board (Top View)

The following are the mechanical properties of the carrier board:

Dimensions	289 cm^2 (170mm x 170mm)
Form Factor	Mini-ITX
Major Interfaces	See Carrier Board Expansion Connectors for details regarding carrier board interfaces

3.9.1 Power and Boot Configuration Switches

Warning! : Before making any changes to the configuration switches, make sure to note down the previous configuration. The default switch settings are above.

3.9.1.1 Dip Switch S10 Configuration Options

There is a DIP switch S10 on the top side of the Open-Q 835 µSOM carrier board. The 8-bit switch allows the user to control the system configuration and boot options. Table 3.8-1 below outlines the pin outs and connections of this DIP switches.

Table 2 Dip Switch S10 HW / SW configuration

Function	DIP Switch	Description	Notes
FORCED_USB_BOOT	S10-1	Toggles between FORCE USB boot and Normal boot. Enables FORCE USB (GPIO 57) when DIP switch is in ON position.	Default out of the box configuration is OFF (Normal boot) **Note:** FORCE USB boot option is for Intrinsyc factory programming use.
CBL_PWR_N	S10-2	Enables APQ to auto boot when power is supplied	Default out of the box configuration is OFF (no auto boot)
BOOT_CONFIG[3]	S10-3	Enables APQ boot configuration 3 when DIP switch turned on. Controlled by APQ GPIO104 See schematic for boot configuration options. NOTE: µSOM boot configurations are not supported on the development kit.	Default out of the box configuration is OFF (boot from UFS)
BOOT_CONFIG[2]	S10-4	Enables APQ boot configuration 2 when DIP switch turned on. Controlled by APQ-GPIO103	Default out of the box configuration is OFF (boot from UFS)
BOOT_CONFIG[1]	S10-5	Enables APQ boot configuration 1 when DIP switch turned on. Controlled by APQ-GPIO 102	Default out of the box configuration is OFF (boot from UFS)
N/C	S10-6	NA	NA
WATCHDOG _DISABLE	S10-7	Enables WATCHDOG_DISABLE when DIP switch turned on. Controlled by APQ-GPIO 101	Default out of the box configuration is OFF (Watchdog enabled)
N/C	S10-8	NA	NA

Figure 6 shows the default DIP switch position.

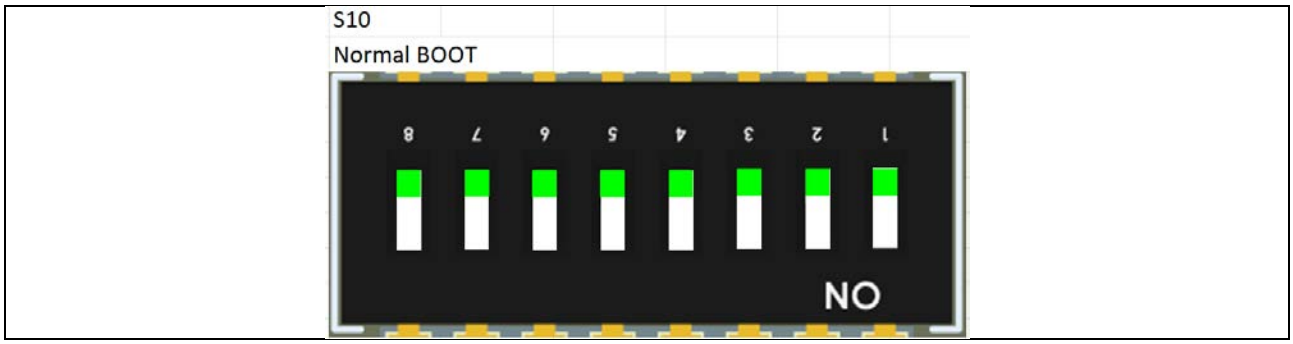


Figure 6 Default Dip Switch S10 Configuration

3.9.1.2 Dip Switch S1 Configuration Options

Table 3 Dip Switch S1 Configuration

Function	DIP Switch	Description	Notes
N/C	S1-1	NA	NA
LCD_AMOLED_SEL	S1-2	Select between LCD or AMOLED Display type. Set to AMOLED display type in OFF position.	Default out of the box configuration is ON Note: This switch function is currently not supported.
BATT_ID_CONN	S1-3	Enables SOM to detect battery presence and battery type via BATT_ID line. • If the supported Battery does not come with BATT_ID, set switch to ON position. • If DC IN source is used, set switch to ON position. • If the supported Battery comes with BATT_ID, set switch to OFF position. Please consult with intrinsyc for specific BATT_ID value.	Default out of the box configuration is ON
BAT_THERM_CONN	S1-4	Enables SOM to detect battery presence and battery temperature via BAT_THERM line. The default battery thermistor is 10k OHM at 25C NTC. • If the supported Battery does not come with BAT_THERM, set switch to ON position. • If DC IN source is used, set switch to ON position. • If the supported Battery comes with BATT_THERM 10KOHM NTC, set switch to OFF position. Please consult with intrinsyc if a different BATT_THERM is used.	Default out of the box configuration is ON

Figure 7 shows the default S1 DIP switch position. The S1 switch is configured to be powered by DC IN.

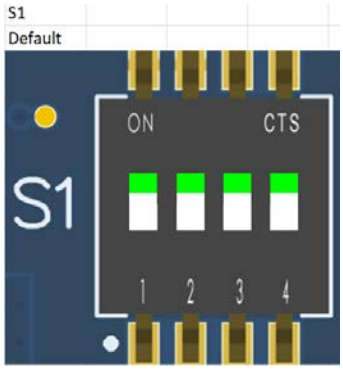


Figure 7 Default DIP Switch S1 Configuration

Figure 8 shows the S1 DIP switch configuration to be powered by an Intrinsyc recommended battery pack.

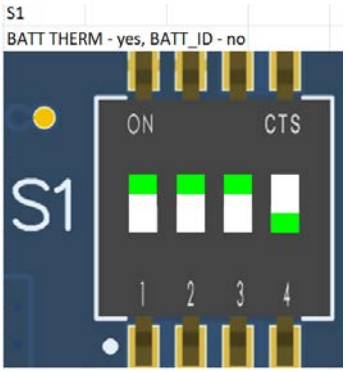


Figure 8 Battery Pack Supplied DIP Switch S1 Configuration

3.9.1.3 Slide Switch S300 Power Source Select Options

The Slide Switch S300 provides the developer option to supply the Dev kit from a DC power source or a battery pack.

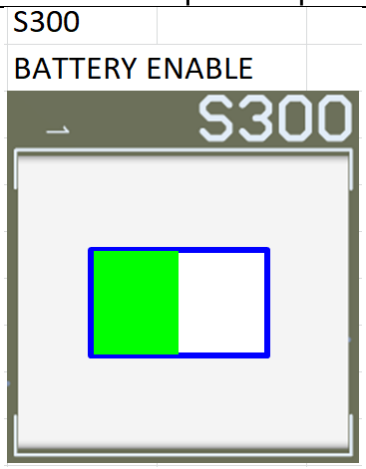
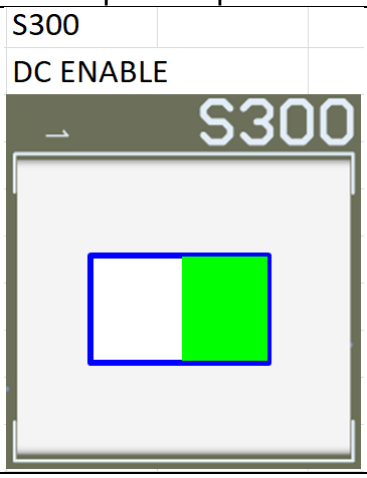
BATTERY PACK to power up the dev kit	DC IN to power up the dev kit.
	

Figure 9 Power Source Select Options

3.9.2 Carrier Board Expansion Connectors

The following table lists the connectors, expansions, LEDs and their usages on the carrier board:

Table 4 Carrier Board Expansion Options and Usage

Domain	Interface	Description	Specification	Usage
uSOM	J800, J801, J900	Board to Board connectors to uSOM	3 x 100-pins Hirose DF40 connectors (B2B Connector).	Expose uSOM signals for CB functions
Power	J21	DC Power Input	12 V DC Power Supply 5 A	Power Supply
	J300	Battery Connector	6 pin header	For Battery operation and charging development
	J60	Power connector	20 pin header	For providing extra current to camera connectors when needed (ie: when high performance cameras used)
	J86	3 pin power probe header	Sense lines connected across 0.005 Ohm resistor	To measure current consumption of µSOM
USB 3.1 Type-C	J23	USB 3.1 via USB Type C	USB 3.1 support, HS, SS, including DP alt	USB 3.1 support, HS, SS, including DP alt
Debug Serial via USB	J22	Debug Serial UART console over USB for development	Vertical USB Micro B connector	Development Serial Connector for debug output via USB

Domain	Interface	Description	Specification	Usage
Power Switch	S300	Power switch between battery and DC	Power Switch	To switch between DC input and Battery input
Buttons	S103	General Purpose SW button	SMD Button	Additional button for general purpose (connected to APQ_GPIO120)
	S100	Power Button	SMD Button	Power Button for Suspend / Resume and Power off
	S101	Volume + key	SMD Button	Volume +Key
	S102	Volume – key	SMD Button	Volume – Key
Sensor IO Connector	J53	24 pin Sensor Expansion Connectors	Support any user sensor card, Standard 24-pin ST Micro PLCC support via optional daughter card	Available via Intrinsyc optional accessories kit
Gen10 connector (bottom side)	J55	Connector for Qualcomm's internal sensor boards	60 pin connector sensor Gen 10	To interface with Qualcomm's internal sensor boards (for Intrinsyc internal use only – not supported) Can be used for other purposes.
MISC Interface Header	J54	20-pin general purpose IO for SPI / I2C / GPIOs/ UIM/ UART functions and other unused GPIOs from PMIC and APQ education header.	Full BLSP1 (SPI/ UART/ I2C/ GPIO) APQ GPIOs MPPs Power	Useful when user wants to use UART GPIOs pins as BLSP other functions (GPIO/ I2C/ UIM/ SPI).
Micro SD (bottom side)	J6	Micro SD card	4bit Micro SD card support	External Storage
ANC Audio Jack	J27	Audio Jack supported using WCD9335	ANC audio jack providing 2lineout and 1 headset drivers (with Qualcomm® ANC technology)	Audio support
3-Digital Microphone via audio input expansion header	J50	Audio expansion Supported using WCD9335	Audio In header	For Digital audio input for Digital MIC, I2S codec, Slim bus interface.
3-Analog Microphone via audio input expansion header	J50	Audio expansion Supported using WCD9335	Audio In header	For Analog audio input for Analog MIC (differential signal)
2-Loud Speaker via audio output expansion header	J26	Audio expansion Supported using WCD9335	Audio Out header	For loud speaker output after signal has been processed

Domain	Interface	Description	Specification	Usage
Earpiece via audio output expansion header	J26	Audio expansion Supported using WCD9335	Audio Out header	For earpiece output after signal has been processed
Haptics Connector	J802	2 pin haptics driver header	Haptics driver output from PMI8998	For connecting a 2 pin vibrating motor
PCI Express Slot	J30	PCI Express for external peripheral connectivity	PCIe1 v2.1 Supports half card only Supports 10W card via power supply Supports 25W card via ATX power supply	To connect an Ethernet PCIe card board to support Ethernet.
CSI Camera connectors	J3, J4, J5	3 x CSI port connector with CLK, GPIOS, CCI	Supports 3 x Camera interfaces via three separate connectors • 3 x MIPI-CSI each 4 lane • External flash driver control • Support for 3D camera configuration • Separate I2C / CCI control MIPI Alliance Specification v1.00 for Camera Serial Interface	To connect to MIPI CSI camera module
Coin Cell Holder(bottom side)	H100	Coin Cell battery(Optional via stuffing)	Coin cell battery for PMIC RTC	RTC
RGB LED	DS1, DS2, DS3	3xLED	Red : PMIC Driven Green: PMIC Driven Blue: PMIC Driven	Red : Charging Green : Charging complete Blue : General Purpose
Power Indication LED	DS4, DS6	2xLED	Green: system power Red: charging status	Green: system power Red: charging
WiFi/BT Antenna	J9	PCB Antenna	2.4 – 5.1 GHz	Antenna to µSOM WiFi/BT port

Domain	Interface	Description	Specification	Usage
WiFi Antenna	J65	PCB Antenna	2.4 – 5.1 GHz	Antenna to µSOM WiFi port
HDMI Port	J25	Extended Display ports	HDMI port supports up to 4K without HDCP 1.4A spec	External Display
LCD Display and Touch connector	J2	100 pin for LCD signals via b2b connector to display adapter board	4-lane MIPI DSI0 , DSI1 I2C/SPI/GPIO Backlight	Can work as one dual DSI or both independent display

The sections below will provide in depth information on each expansion header and connector on the carrier board. The information listed below is of particular use for those who want to interface other external hardware devices with the Open-Q 835 µSOM. Before connecting anything to the development kit, please ensure the device meets the specific hardware requirements of the processor.

3.9.2.1 uSOM Connector J800/J801/J900

The complete Open-Q 835 µSOM development kit comes with a uSOM and a Carrier Board (CB). Three DF40 board to board connectors are used in the design to bring out the critical signals from the uSOM to the carrier board for different functional blocks.

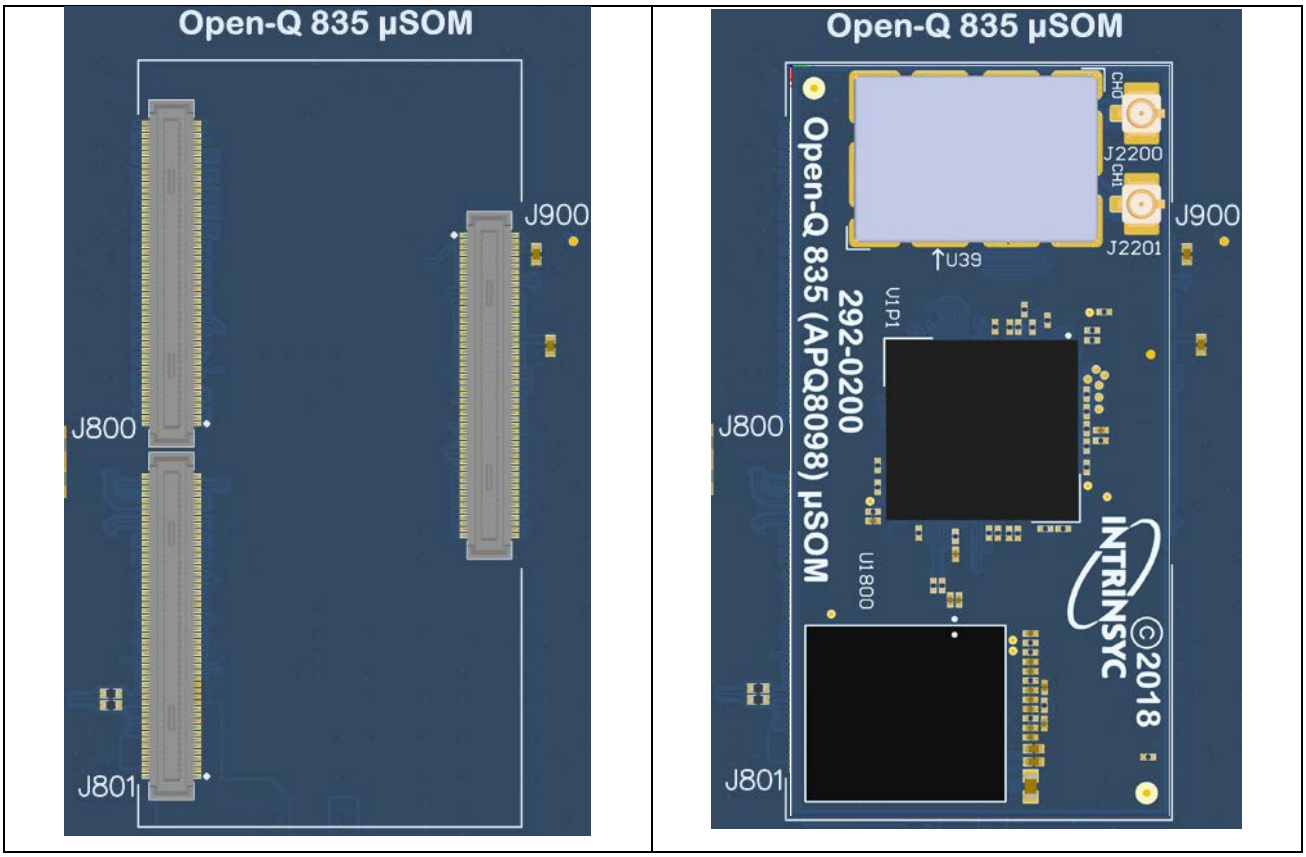


Figure 10 J800, J801, J900 uSOM Board to Board Connectors

3.9.2.2 DC Power Input J21

The Open-Q 835 µSOM development kit power source connects to the 12V DC power supply jack J21. Starting from the power jack, the 12V power supply branches off into different voltage rails via step down converters on the carrier board and PMIC on the µSOM. The µSOM is powered by 3.8V via a Texas Instrument step down converter U400 on the carrier board. To ensure the µSOM is getting powered correctly, user can monitor the current going into the µSOM via the power probe header J86 (see section below).

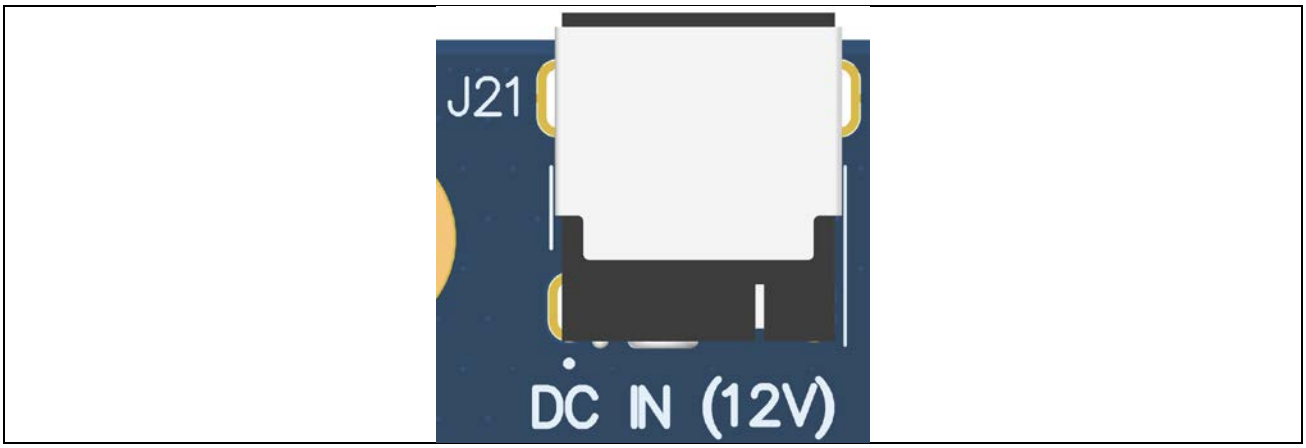


Figure 11 J21 12V DC Power Jack

The µSOM consists of 3 PMIC modules. Functionalities of the 3 PMICs are outlined below.

PMI8998 PMIC is used for:

- Source various regulated power rails
- Battery charging with Type-C support. Please see section below for additional information on battery support.
  Please note that support for battery charging over external charger is not implemented in the design. Please contact Intrinsyc for such customization.
- Display bias and backlight
- RGB indicator LED driver

PM8998 PMIC is used for:

- Primary core PMIC
- Source system power and main power rails
- Source system clock

PM8005 PMIC is used for:

- Secondary core PMIC
- Source system power rails from opposite side of the processor for layout optimization

3.9.2.3 Battery Header J300

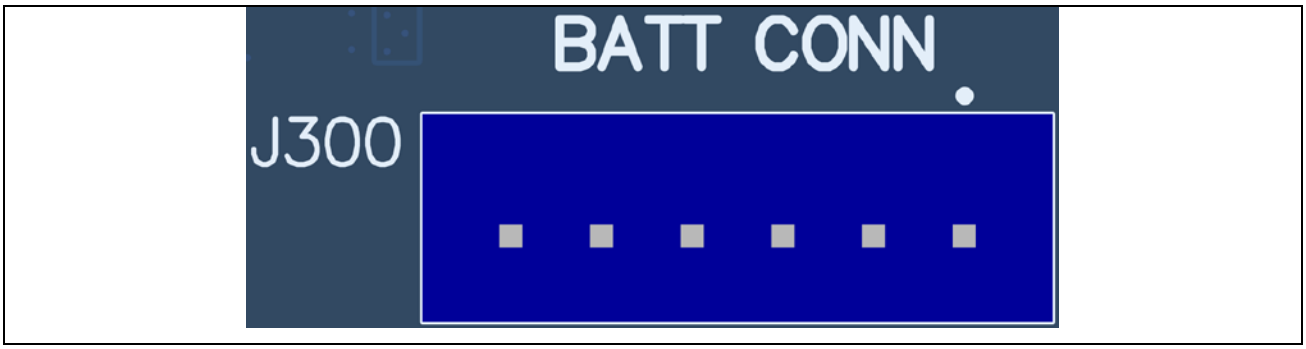


Figure 12 J300 Battery Header

The Open-Q µSOM 835 development platform can also power the µSOM with a single cell Lithium-Ion Polymer (LiPo) battery pack which connects to header J300. The purpose of this header is to be used by the end user to develop a battery charging solution, including battery characterization. Intrinsyc recommends using the AA Portable Power Corp's CU-J479-V2 / 1ICP7/55/85 Lithium ion battery pack. This is a single cell pack with a nominal voltage of 3.8V and a capacity of 3200mAh (11.8 Wh, 5A rate). If user intends to use a different battery, please note the pin outs on this battery header.

Table 5 Battery Header J300 Pin out

Description	Signal	Pin	Note
µSOM Battery positive supply terminal	VBAT Plus (VBAT+)	J300[1]	
µSOM Battery positive supply terminal	VBAT Plus (VBAT+)	J300[2]	
N/C	N/C	J300[3]	
Internal battery pack temperature	BATT_THERM (The recommended battery has a 10K Ohm thermistor)	J300[4]	
µSOM Battery negative supply terminal	VBAT Minus(VBAT-)	J300[5]	
µSOM Battery negative supply terminal	VBAT Minus(VBAT-)	J300[6]	

Please note that the battery only powers the µSOM. To ensure proper functionality of the development kit, the 12V power supply must be attached at J21. When a battery is not in use, the TI step down converter U400 is used to power the µSOM.

3.9.2.4 Power Header via 20 Pin Connector J60

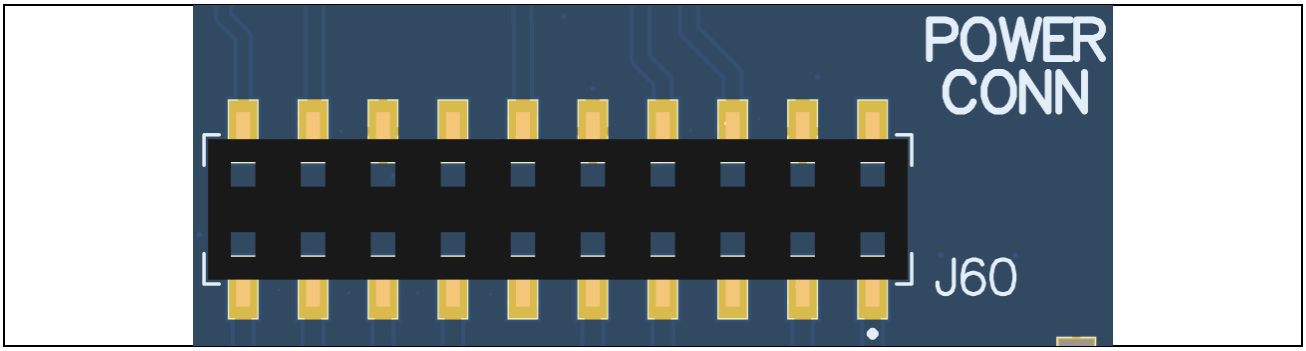


Figure 13 J60 Power Connector

- For providing camera connectors with additional current than what is originally supported by on board regulators. This is to mitigate the effect of high resistance and IR drop on flat cables which can violate camera sensor requirements for high performance cameras
- It is recommended to use this when high performance (high mega pixels) cameras are being used. Usually high-performance cameras require more power
- Can also be used as a general power header if user would like to use voltage rails brought out by connector

Table 6 Power Header J60 Pin out

Description	Signal	Pin NO		Description	Signal	Pin NO
1.12V power rail for camera 0	MB_ELDO_CAM0_DVDD	J60[1]		2.85V power rail for camera (AVDD)	VREG_L22A_2P85	J60[2]
2.8V power rail for camera 0 (VDD)	MB_ELDO_CAM0_VCM	J60[3]		GND	GND	J60[4]
1.8V power rail for camera 0, 1, 2	VREG_LVS1A_1P8	J60[5]		3.3V power rail for camera 0, 1, 2	MB_VREG_3P3	J60[6]
1.12V power rail for camera 1	MB_ELDO_CAM1_DVDD	J60[7]		2.85V power rail for camera 1 (AVDD)	MB_ELDO_CAM_AVDD	J60[8]
2.7V rail from PMIC	VREG_L16_2P7	J60[9]		GND	GND	J60[10]
1.8V power rail for camera 0, 1, 2	VREG_LVS1A_1P8	J60[11]		3.3V power rail for camera 0, 1, 2	MB_VREG_3P3	J60[12]
1.12V power rail for camera 2	MB_ELDO_CAM2_DVDD	J53[13]		2.85V power rail for camera (AVDD)	VREG_L22A_2P85	J60[14]
2.8V power rail for camera 0, 2 (VDD)	MB_ELDO_CAM2_VCM	J53[15]		GND	GND	J60[16]
1.8V power rail for camera 0, 1, 2	VREG_LVS1A_1P8	J60[17]		3.3V power rail for camera 0, 1, 2	MB_VREG_3P3	J60[18]
5V power rail for camera 0, 1, 2	MB_VREG_5P0	J60[19]		12V power rail for camera 0, 1, 2	DC_IN_12V	J60[20]

3.9.2.5 Power Probe Header J86

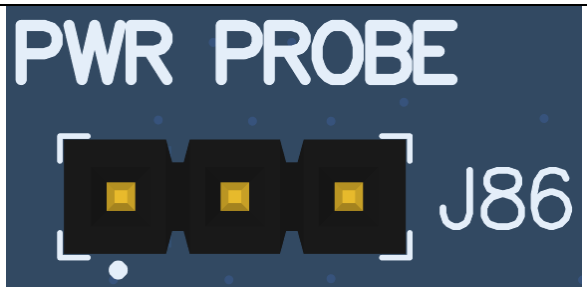


Figure 14 J86 Power Probe Header

The power probe header is used to sense/ monitor the current on the 3.8V power rail going into the µSOM. The table below summarizes the pin outs of header J86.

Table 7 Power Probe Header J86 Pin out

Description	Signal	Pin
µSOM power positive current sense line	SOM_PWR_SENSE_P	J86[1]
µSOM power negative current sense line	SOM_PWR_SENSE_N	J86[2]
GND	GND	J86[3]

To obtain power consumption measurements, the header is connected to a data acquisition unit (e.g. Keithley 2701) and the voltages on the SOM_PWR_SENSE_P/N pins are captured every few seconds over the test period (typically 30 minutes). The SOM power consumption is then calculated as (where R_{SENSE} = 5 milliohms):

$$P_{SOM} = V_{SOM\_PWR\_SENSE\_N} * \frac{(V_{SOM\_PWR\_SENSE\_P} - V_{SOM\_PWR\_SENSE\_N})}{R_{SENSE}}$$

3.9.2.6 USB Type C J23

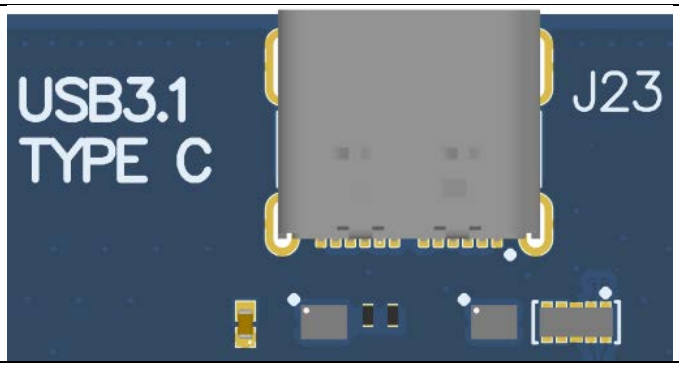


Figure 15 J23 USB Type C

The USB Type C connector on the carrier board supports USB3.1(HS/SS), DP alt function, and dual role power/charging mode operations.
The same USB Type C connector is used for android debug bridge (ADB) access.

3.9.2.7 Debug Serial UART over USB J22

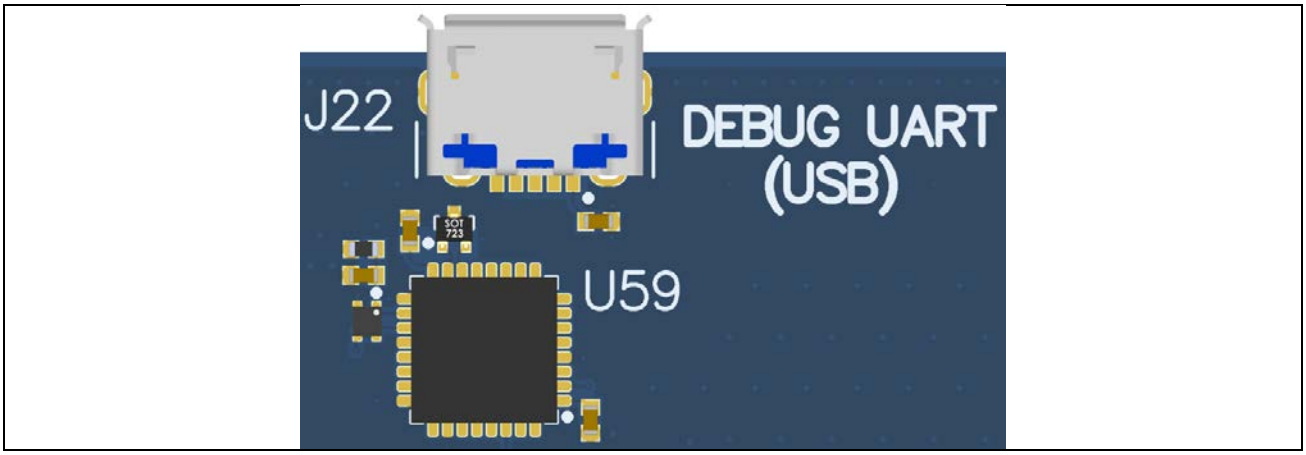


Figure 16 J22 Debug UART over USB

The UART connection used on the Open-Q 835 µSOM is a USB micro B connector (J22). This debug UART is available over USB via the FTDI FT232RQ chip on the carrier board. To get the serial terminal working with a PC, user needs to ensure that the appropriate FTDI drivers are installed.

3.9.2.8 Carrier Board Buttons

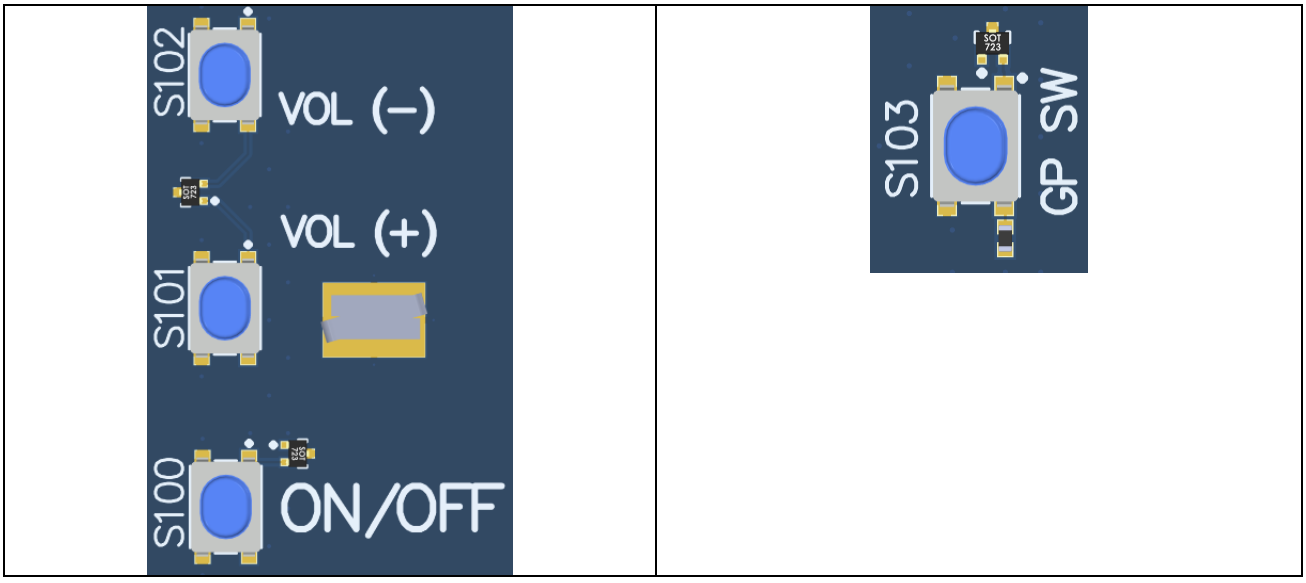


Figure 17 J22 Debug UART over USB

There are total of four push buttons on the Carrier Board. S100, S101, S102, S103 are defined as Power, Volume+, Volume-, and General-Purpose buttons.
Volume- is the default button to enter fastboot for development.

3.9.2.9 Sensor IO Expansion Header J53

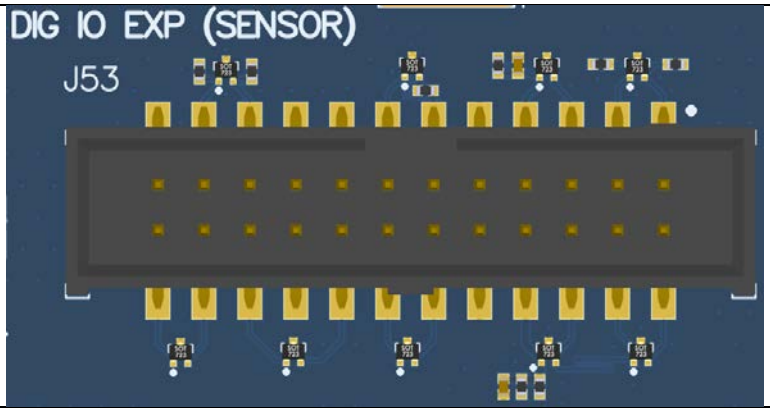


Figure 18 J53 Sensor Expansion Header

The sensor expansion header J53 allows for a 24-pin connection to an optional sensor board.

Following is the pin breakout for sensor expansion header J53.

Table 8 Sensor Expansion Header J53 Pin out

Description	Signal	Pin NO		Description	Signal	Pin NO
SSC I2C-3 serial data (1.8V)	SSC_I2C_3_SDA	J53[1]		Accelerometer interrupt input to processor via GPIO117 (1.8V)	ACCEL_INT_N	J53[2]
SSC I2C-3 serial clock (1.8V)	SSC_I2C_3_SCL	J53[3]		Cap interrupt input to processor via GPIO123 (1.8V)	CAP_INT_N	J53[4]
Sensor reset signal from processor to sensor via GPIO80 (1.8V)	MEMS_RESET_N	J53[5]		Gyroscope interrupt input to processor via GPIO118 (1.8V)	GYRO_INT	J53[6]
Sensor IO PWR 1.8 V VREG_LVS2A_1P8 power supply regulator (Digital)	SENS_IO_PWR	J53[7]		Sensor Analog power supply from VREG_L19A 2.85V or 3.3V (If R160 populated)	SENS_ANA_PWR	J53[8]
GND	GND	J53[9]		GND	GND	J53[10]
HRM interrupt/ configurable GPIO122 (1.8V)	HRM_INT	J53[11]		Touch screen interrupt input from processor via GPIO125 (1.8V)	TS_INT0	J53[12]

Description	Signal	Pin NO		Description	Signal	Pin NO
SSC SPI-1 chip select 2 (1.8V)	SSC_SPI_1_CS1 _MAG_N	J53[13]		Alternate sensor interrupt input to processor via GPIO120 (1.8V)	ALSPG_INT_N	J53[14]
NC	NC	J53[15]		Digital Compass interrupt input to processor via GPIO119 (1.8V)	MAG_DRDY_INT	J53[16]
NC	NC	J53[17]		NC	NC	J53[18]
SSC SPI-1 chip select 1 (1.8V)	SSC_SPI_1_CS_ N	J53[19]		SSC SPI-1 data master out/ slave in (1.8V)	SSC_SPI_1_MOSI	J53[20]
SSC SPI-1 clock (1.8V)	SSC_SPI_1_CLK	J53[21]		SSC SPI-1 data master in/ slave out (1.8V)	SSC_SPI_1_MISO	J53[22]
NC	NC	J53[23]		SSC power enable (1.8V)	SSC_PWR_EN	J53[24]

Please note that these SSC sensor ports should only be used with Intrinsyc supported sensors. Please consult with Intrinsyc support for sensor selection.

Note that there is an unpopulated Gen-10 connector header (J55) footprint at the bottom of the carrier board. Install the Samtec (part number: QSH-030-01-L-D-A) connector here if needed.

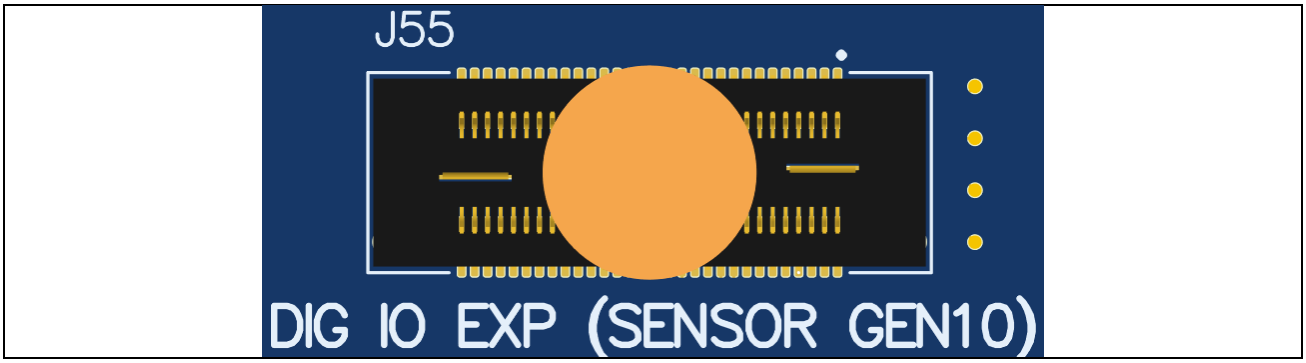


Figure 19 J55 Gen-10 Sensor Connector (Samtec QSH-030 series)

3.9.2.10 MISC Interface header J54

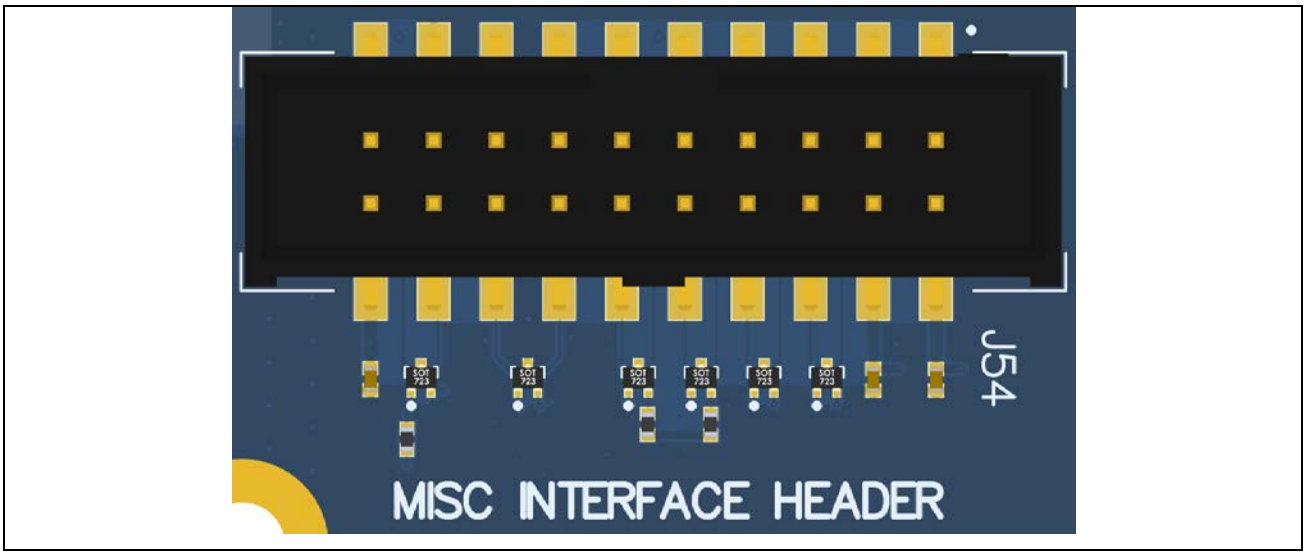


Figure 20 J54 Education / GPIO header

MISC Interface GPIO header expansion J54 is a 20-pin connector that provides access to BLSP1 and MI2S signals. It is ideally used for connecting external peripherals such as microcontrollers and any other devices that are based on I2C, SPI, UART, UIM and GPIO. The following are the detailed pin out information for MISC Interface header J54.

Table 9 MISC Interface Expansion Header J54 Pin Out

Description	Signal	Pin NO		Description	Signal	Pin NO
NC	NC	J54[1]		VREG_S4A 1.8V voltage regulator max 150mA	VREG_S4A_1P8	J54[2]
SPI interface, BLSP1_SPI_MOSI (1.8V)	BLSP1_SPI_MOSI (APQ-GPIO0)	J54[3]		MB_VREG_3P3 (Default 3.3V Power Supply) max 300mA	MB_VREG_3P3	J54[4]
SPI interface, BLSP1_SPI_MISO(1.8V)	BLSP1_SPI_MISO (APQ-GPIO1)	J54[5]		I2S Interface, word select, QUA_MI2S_WS (1.8V)	QUA_MI2S_WS (APQ-GPIO59)	J54[6]
SPI interface, BLSP1_SPI_CS_N(1.8V)	BLSP1_SPI_CS_N (APQ-GPIO2)	J54[7]		LNBB_CLK2 Configurable Low Noise BaseBand Clock	LNBB_CLK2	J54[8]
SPI interface, BLSP1_SPI_CLK (1.8V)	BLSP1_SPI_CLK (APQ-GPIO3)	J54[9]		I2S Interface, Serial Clock, QUA_MIS2_SCK (1.8V)	QUA_MIS2_SCK	J54[10]
NC	N/C	J54[11]		I2S Interface, Data0, QUA_MI2S_DATA0 (1.8V)	QUA_MI2S_DATA0	J54[12]

Description	Signal	Pin NO		Description	Signal	Pin NO
NC	N/C	J54[13]		I2S Interface, Data1, QUA_MI2S_DATA 1 (1.8V)	QUA_MI2S_DATA 1	J54[14]
NC	N/C	J54[15]		I2S Interface, Data2, QUA_MI2S_DATA 2 (1.8V)	QUA_MI2S_DATA 2	J54[16]
GND	GND	J54[17]		I2S Interface, Data3, QUA_MI2S_DATA 3 (1.8V)	QUA_MI2S_DATA 3	J54[18]
Boot Config, FORCE_USB_BOOT	FORCE_USB_BOOT (APQ-GPIO57)	J54[19]		5V power supply max 150mA	MB_VREG_5P0	J54[20]

3.9.2.11 Micro SD Card Holder J6

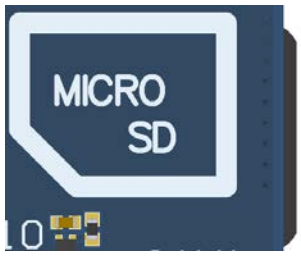
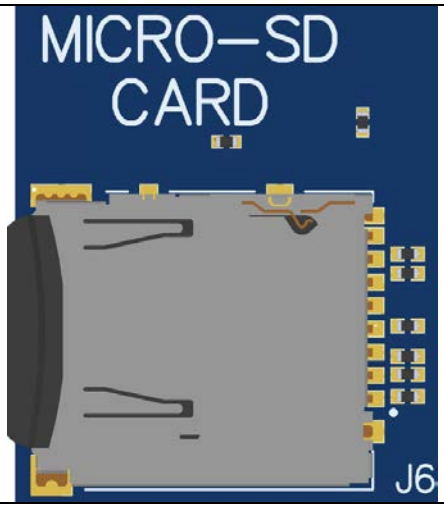
Top View	Bottom View
	

Figure 21 J6 Micro SD Card Holder

Micro SD Card holder is located on the bottom side of the Carrier Board. J6 is a push/push type holder.

3.9.2.12 ANC Headset Jack J27

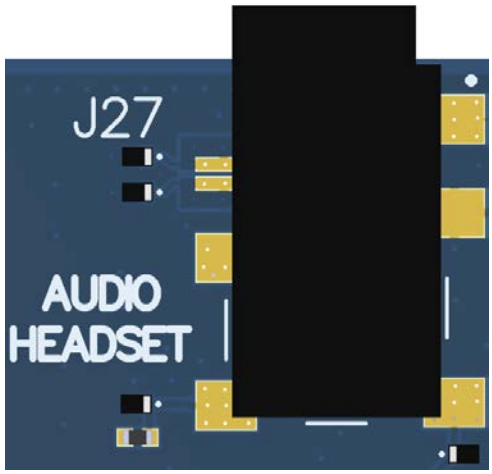


Figure 22 ANC Headphone Jack

The ANC headset jack (J27) is a special 3.5mm TRRS jack with ANC capabilities. It is backwards compatible with standard headset jacks.

3.9.2.13 Audio Inputs Expansion Header J50

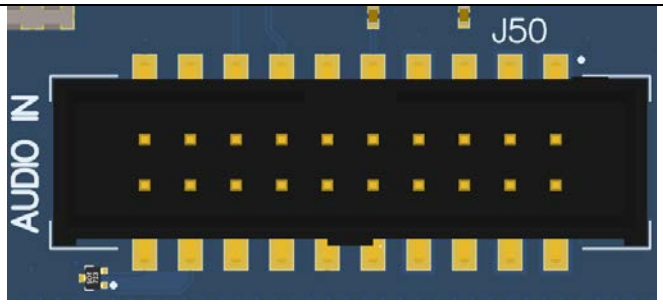


Figure 23 J50 Audio Inputs Expansion Header

This header expansion provides the following audio inputs:

1. 3 digital mic inputs (each can support 2 digital microphones)
2. 3 analog mics
3. Voltage rails to support analog and digital mics

The table below outlines the pin out information of the audio inputs expansion header J50:

Table 10 Audio Inputs Expansion Header J50 Pin out

Description	Signal	Pin NO		Description	Signal	Pin NO
Analog MIC1 positive differential input	CDC_IN1_P	J50[1]		Analog MIC1 negative differential input	CDC_IN1_N	J50[2]
Analog MIC5 positive differential input	CDC_IN5_P	J50[3]		Analog MIC5 negative differential input	CDC_IN5_N	J50[4]
MIC bias output voltage 1	MIC_BIAS1	J50[5]		MIC bias output voltage 3	MIC_BIAS3	J50[6]
Analog MIC6 positive differential input	CDC_IN6_P	J50[7]		Analog MIC6 negative differential input	CDC_IN6_N	J50[8]
MIC bias output voltage 4	MIC_BIAS4	J50[9]		3.3V power supply max 500mA	MB_VREG_3P3	J50[10]
GND	GND	J50[11]		GND	GND	J50[12]
Clock for digital MIC 1 and 2	CDC_DMIC_CLK0	J50[13]		Clock for digital MIC 3 and 4	CDC_DMIC_CLK1	J50[14]
Digital MIC 1 and 2 data line	CDC_DMIC_DATA0	J50[15]		Digital MIC 3 and 4 data line	CDC_DMIC_DATA1	J50[16]
1.8V power supply max 300mA	VREG_S4A_1P8	J50[17]		Clock for digital MIC 5 and 6	CDC_DMIC_CLK2	J50[18]
GND	GND	J50[19]		Digital MIC 5 and 6 data line	CDC_DMIC_DATA2	J50[20]

3.9.2.14 Audio Outputs Expansion Header J26

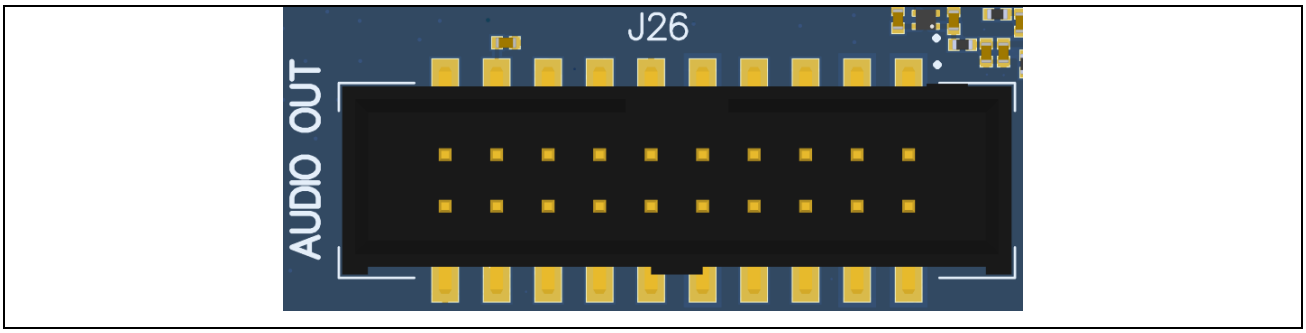


Figure 24 J26 Audio Outputs Expansion Header

This header expansion provides the following audio outputs:

1. 2 differential analog audio line out
2. 2 single ended analog audio line out
3. 1 differential analog earpiece amplifier output (no external amp needed)
4. 2 speaker amplifier enable control
5. Voltage rails to support analog and digital mics

The table below outlines the pin out information of the audio outputs expansion header J26:

Table 11 Audio Outputs Expansion Header J26 Pin out

Description	Signal	Pin NO		Description	Signal	Pin NO
Analog audio line out 1, positive differential output	CDC_LINE_OUT1_P	J26[1]		Analog audio line out 1, negative differential output	CDC_LINE_OUT1_N	J26[2]
Analog audio line out 2, positive differential output	CDC_LINE_OUT2_P	J26[3]		Analog audio line out 2, negative differential output	CDC_LINE_OUT2_N	J26[4]
Audio line outputs 3 and 4 GND reference	CDC_LINE_REF	J26[5]		3.3V output power supply	MB_VREG_3P3	J26[6]
Analog audio line out 3, single ended output	CDC_LINE_OUT3	J26[7]		Analog audio line out 4, single ended output	CDC_LINE_OUT4	J26[8]
Analog earpiece amplifier out, positive differential output	CDC_EAR_P	J26[9]		Analog earpiece amplifier out, negative differential output	CDC_EAR_N	J26[10]
GND	GND	J26[11]		3.8V system power supply	SOM_SYS_PWR_PER	J26[12]
Digital soundwire data for WSA8810/ WSA8815 smart speaker amplifier	CDC_SWR_CLK	J26[13]		Digital soundwire data for WSA8810/ WSA8815 smart speaker amplifier	CDC_SWR_DATA	J26[14]

Description	Signal	Pin NO		Description	Signal	Pin NO
APQ GPIO_96	APQ_GPIO96	J26[15]		Speaker amplifier enable 2	SPKR_AMP_EN2	J26[16]
1.8V output power supply	VREG_S4A_1P8	J26[17]		12V output power supply	DC_IN_12V	J26[18]
5.0V output power supply	MB_VREG_5P0	J26[19]		GND	GND	J26[20]

3.9.2.15 Haptic Driver Header J802

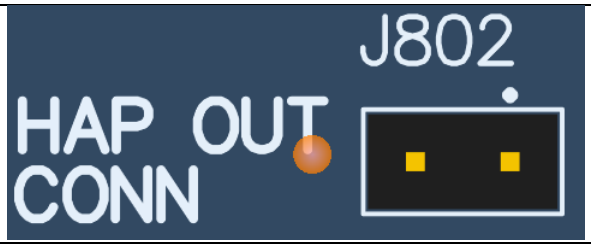


Figure 25 J802 Haptic Driver Header

The Carrier Board supports a 2 pin Haptics driver output from PMI8998. The header can be connected to a Linear Resonant Actuator (LRA) or an Eccentric Rotating Mass ERM motor and the driver voltage is configurable from 1.2V to 3.6V.

3.9.2.16 PCI Express 1X Slot J30

The PCI Express slot J30 used on the Open-Q 835 µSOM development kit is a standard PC style half card slot. It allows for external peripheral connectivity such as Gigabit Ethernet, Gigabit Wi-Fi, PCIe based audio / video processors etc. Since there is no native Ethernet connectivity on the Open-Q platform, an off-the shelf PCIe based Ethernet card can be used here. Please check the software compatibility before connecting the PCIe Ethernet card. In addition to being able to establish external connectivity, the connector provides access to the PCIE interface which is being routed out from the µSOM.

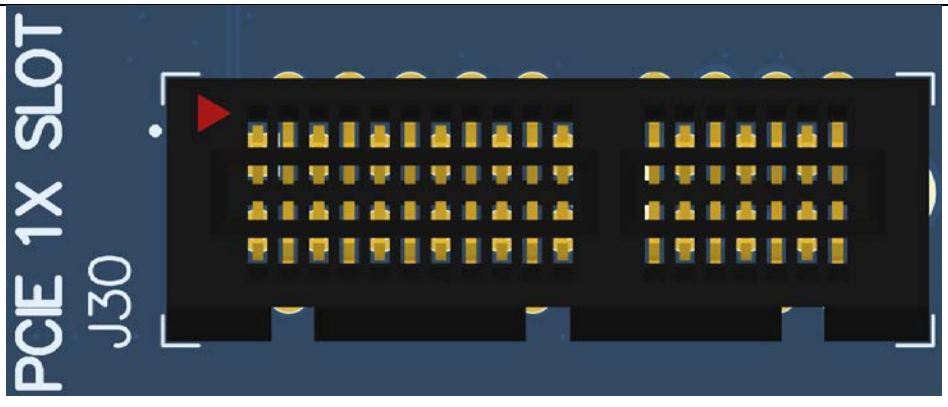


Figure 26 J30 PCIe Connector

- PCI slot power specification
    - Supports half card only
    - Supports 10W card via PSU

Power Rail	Low Power	High Power
3.3 V ± 9%	3 A Max	3A Max
12 V ± 8%	0.5 A Max	2.1 A max
3.3 Vaux ± 9%	375mA Max	375mA Max

- PCIe card Mechanical Specifications:
    - Card length:
        - Half card: 6.6” (167.65mm)
        - Full size card: > 7.0” (177.8mm) (This will not support mini ITX)
    - Card height:
        - Standard: 4.2” (106.7mm)
        - Low profile: 2.536” (64.4mm)

3.9.2.17 Camera Connectors

The Open-Q 835 µSOM development kit supports three 4-lane MIPI CSI camera interfaces via three separate JAE 41-pin connectors.

The following are some features of the camera connectors:

- 3 x 4 lane MIPI CSI signals
- No support for integrated flash driver
- Two separate I2C controls (CCI0, CCI1) if needed
- Supports all CSI interfaces
- All camera CSI connectors are on the carrier board edge
- Self-regulated camera modules can be powered with 3.3V power (MB_VREG_3P3)
- Uses JAE FI-RE41S-VF connector for exposing MIPI, CLK, GPIOs and Power rails.
- Please use JAE FI-RE41S-HF to mate with the camera connectors on the carrier board

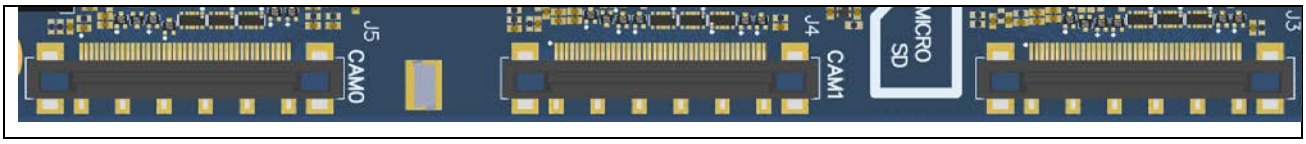


Figure 27 Camera Connectors (J5, J4, J3)

The figure above shows the three MIPI CAM0 (J5), CAM1 (J4) and CAM2 (J3) connectors. The table below outlines the pin outs of these connectors

Table 12 MIPI CSI Camera Connector Pinouts (J5,J4,J3)

Pin#	CAM0 (J5)	CAM1 (J4)	CAM2 (J3)	Description
1, 2, 3	MB_VREG_3P3	MB_VREG_3P3	MB_VREG_3P3	Power output. Connected to main +3.3V MB_VREG_3P3 max current 700mA
4	GND	GND	GND	Ground
5	VREG_L22A_2P8	MB_ELDO_CAM_AVDD	MB_ELDO_CAM_AVDD	Power output. Connected to PM8998 VREG_L17A and on board LDO 2.8V. Default is +2.8V. Maximum current 300mA
6	MB_ELDO_CAM0_DVDD	MB_ELDO_CAM1_DVDD	MB_ELDO_CAM2_DVDD	Power output. Connected to U5, U6, and U71 AMS LDO regulator. Default is +1.12V. Maximum current 1A
7, 8	MB_ELDO_CAM0_VCM	MB_ELDO_CAM1_VCM	MB_ELDO_CAM2_VCM	Power output. Connected to on board LDO. Default is 2.8V and maximum current is 300mA
9, 10	VREG_LVS1A_1P8	VREG_LVS1A_1P8	VREG_LVS1A_1P8	Power output. Connected to PM8998 VREG_LVS1A switch output. Default is +1.8V. Maximum current 300mA
11	GND	GND	GND	Ground
12	FLASH_STROBE_EN (APQ_GPIO21)	FLASH_STROBE_EN (DNP) (APQ_GPIO21) Install R36 to access signal	FLASH_STROBE_EN (DNP) (APQ_GPIO21) Install R42 to access signal	Output. Connected to APQ8098 Default use is for camera flash strobe enable
13	CAM0_RST_N (APQ_GPIO30)	CAM1_RST_N (APQ_GPIO28)	CAM2_RST_N (APQ_GPIO9)	Output. Connected to APQ8098 GPIO30 / GPIO28/GPIO9. Default use is for camera reset
14	CAM0_STANDBY_N (APQ_GPIO29)	CAM1_STANDBY_N (APQ_GPIO27)	CAM2_STANDBY_N (APQ_GPIO8)	Output. Connected to APQ8098 GPIO29 / GPIO27/GPIO8. Default use is for camera standby
15	CCI_I2C_SCL0 (APQ_GPIO18)	CCI_I2C_SCL0 (APQ_GPIO18)	CCI_I2C_SCL0 (APQ_GPIO18)	Output. Connected to APQ8098 GPIO18. Default use is for camera CCI0 I2C clock interface
16	CCI_I2C_SDA0 (APQ_GPIO17)	CCI_I2C_SDA0 (APQ_GPIO17)	CCI_I2C_SDA0 (APQ_GPIO17)	Input / output. Connected to APQ8098 GPIO17. Default use is for camera CCI0 I2C data interface

Pin#	CAM0 (J5)	CAM1 (J4)	CAM2 (J3)	Description
17	CAM_MCLK0 (APQ_GPIO13)	CAM_MCLK1 (APQ_GPIO14)	CAM_MCLK2 (APQ_GPIO15)	Output. Connected to APQ8098 GPIO13 / GPIO14 / GPIO15. Default use is for camera master clock. Maximum 24MHz
18	FLASH_STROBE_TRIG (APQ_GPIO22)	FLASH_STROBE_TRIG (DNP) (APQ_GPIO22) Install R37 to access signal	FLASH_STROBE_TRIG (DNP) (APQ_GPIO22) Install R43 to access signal	Output. Connected to APQ8098 GPIO25. Default use is for camera flash strobe trigger
19	GND	GND	GND	Ground
20	MIPI_CSI0_LANE0_N	MIPI_CSI1_LANE0_N	MIPI_CSI2_LANE0_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 0
21	MIPI_CSI0_LANE0_P	MIPI_CSI1_LANE0_P	MIPI_CSI2_LANE0_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 0
22	GND	GND	GND	Ground
23	MIPI_CSI0_CLK_N	MIPI_CSI1_CLK_N	MIPI_CSI2_CLK_N	Input. MIPI CSI0 / CSI1 / CSI2 clock lane
24	MIPI_CSI0_CLK_P	MIPI_CSI1_CLK_P	MIPI_CSI2_CLK_P	Input. MIPI CSI0 / CSI1 / CSI2 clock lane
25	GND	GND	GND	Ground
26	MIPI_CSI0_LANE1_N	MIPI_CSI1_LANE1_N	MIPI_CSI2_LANE1_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 1
27	MIPI_CSI0_LANE1_P	MIPI_CSI1_LANE1_P	MIPI_CSI2_LANE1_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 1
28	GND	GND	GND	Ground
29	MIPI_CSI0_LANE2_N	MIPI_CSI1_LANE2_N	MIPI_CSI2_LANE2_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 2
30	MIPI_CSI0_LANE2_P	MIPI_CSI1_LANE2_P	MIPI_CSI2_LANE2_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 2
31	GND	GND	GND	Ground
32	MIPI_CSI0_LANE3_P	MIPI_CSI1_LANE3_P	MIPI_CSI2_LANE3_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 3
33	MIPI_CSI0_LANE3_N	MIPI_CSI1_LANE3_N	MIPI_CSI2_LANE3_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 3
34	GND	GND	GND	Ground
35	CCI_I2C_SDA1 (APQ_GPIO19)	CCI_I2C_SDA1 (APQ_GPIO19)	CCI_I2C_SDA1 (APQ_GPIO19)	Output / Input. Connected to APQ8098 GPIO19. Default use is for camera CCI1 I2C data interface
36	CCI_I2C_SCL1 (APQ_GPIO20)	CCI_I2C_SCL1 (APQ_GPIO20)	CCI_I2C_SCL1 (APQ_GPIO20)	Output. Connected to APQ8098 GPIO20. Default use is for camera CCI1 I2C clock interface
37	CAM_IRQ (APQ_GPIO24)	CAM_IRQ (DNP) (APQ_GPIO24) Install R40 to access signal	CAM_IRQ (DNP) (APQ_GPIO24) Install R46 to access signal	Input. Connected to APQ8098 GPIO24. CAM_IRQ signal
38	CAM0_MCLK3 (DNP) (APQ_GPIO16) Install R16 to access signal	CAM1_MCLK3 (APQ_GPIO16)	CAM2_MCLK3 (DNP) (APQ_GPIO16) Install R47 to access signal	Output. Connected to APQ8098 GPIO16. Use is for secondary camera master clock. Maximum 24MHz

Pin#	CAM0 (J5)	CAM1 (J4)	CAM2 (J3)	Description
39	MB_ELDO_CAM0_DVDD	MB_ELDO_CAM1_DVDD	MB_ELDO_CAM2_DVDD	Power output. Connected to U5, U6, and U71 AMS LDO regulator. Default is +1.12V. Maximum current 1A
40, 41	MB_VREG_5P0 (DNP) Install R10 to access rail	MB_VREG_5P0 (DNP) Install R28 to access rail	MB_VREG_5P0 (DNP) Install R35 to access rail	Power output. 5V Power supply. Maximum 700mA

Note: A connection from the camera connectors on the carrier board to the Intrinsyc camera adapter board is established by a 41-pin cable assembly from JAE Electronics (part number JF08R0R041020MA)

The following table shows the combinations of camera usage for different use cases

Table 13 MIPI CSI Camera Use Cases

CSI PHY	Use case	Comment
CSI0	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 1	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 2	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI0 + CSI1 + CSI2	Up to 4 lane	Three 4-lane CSI (4+4+4 or 4+4+2+1)
CPHY		Three 3-trio CPHY1.0 Note: CPHY is supported by APQ8098 PHY design, but PCB layout is routed for DPHY configuration

3.9.2.18 Coin Cell Battery Holder H100

The coin cell holder option (not populated by default) allows the user to use a coin cell to supply RTC power. It is recommended that a Panasonics ML621 series rechargeable coin cell be used.

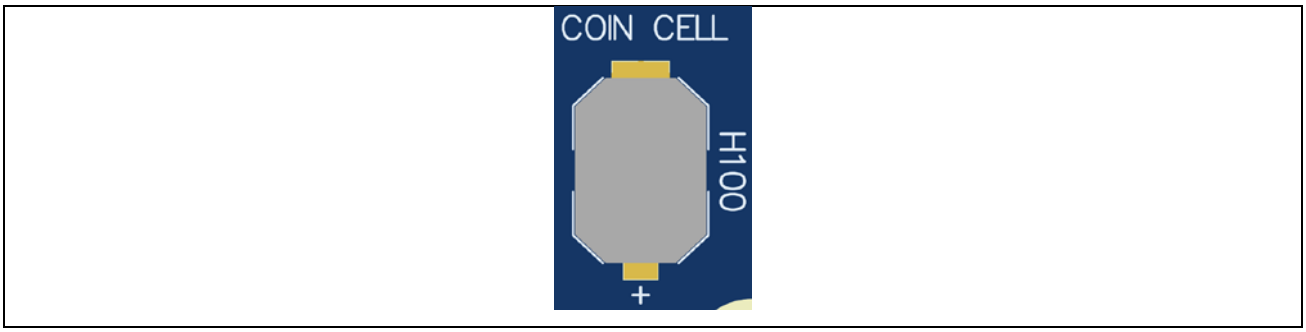


Figure 28 Coin Cell Battery Holder H100

3.9.3 Carrier Board LEDs

There are total of two power indication LEDs and three PMIC driven LEDs on the Open-Q 835 uSOM carrier board.

Power indicator	User LEDs
	

Figure 29 Carrier Board LEDs

Below table lists each LED's default usage:

	LED	**Function**
DS4	Green LED	System power rail is up
DS6	Red LED	Charging status (NOTE: not functional in REV1 of carrier board)
DS1	Red LED	PMIC driven LED – charging
DS2	Blue LED	PMIC driven LED – general purpose
DS3	Green LED	PMIC driven LED – charging complete

3.9.4 Carrier Board WLAN Antenna

The Open-Q 835 µSOM carrier board has two on-board WLAN PCB antennas that are designed to connect to the WCN3990 Wi-Fi module on the µSOM via coaxial cables with U.FL connectors.

Table 14 Carrier Board WLAN Antenna and Usage

Domain	Interface	Description	Specification	Usage
WiFi/BT Antenna	J9	PCB Antenna	2.4 – 5.1 GHz	Antenna to µSOM Wi-Fi/BT port
WiFi Antenna	J65	PCB Antenna	2.4 – 5.1 GHz	Antenna to µSOM Wi-Fi port

These antennas connect to the µSOM in the following configuration:

- WLAN1/BT on the carrier board connects to CH0 on the uSOM
- WLAN0 on the carrier board connects to CH1 on the uSOM

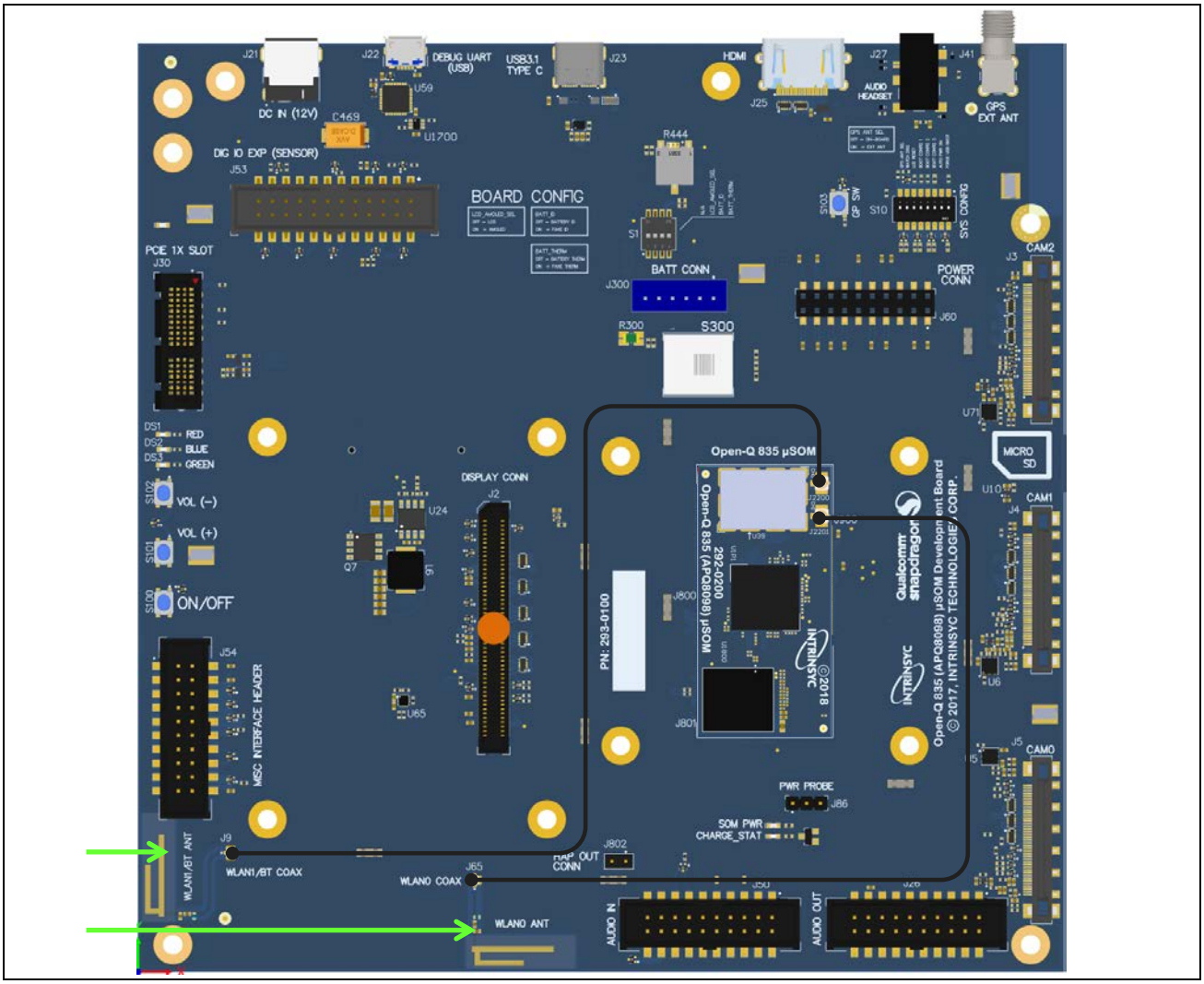


Figure 30 On Board PCB Antennas

3.9.5 Open-Q Display Interface

The display output options for the Open-Q 835 µSOM Development Kit consists of:

- An HDMI type A connector
  - HDMI 2.0 (4K60) or 4K30 Miracast
- USB Type-C Display Port alternate function
- A 100-pin display connector J2 that supports:
  - Dual DSI DPHY 1.2 (up to 3840 x 2400 at 60 fps)
  - Touch screen capacitive panel via I2C or SPI, and interrupts (up to one device)
  - Backlight LED
    - Can support external backlight driver control and power
    - PMI8998 backlight driver supports three LED strings of up to 30mA each with 28V maximum boost voltage

Domain	Interface	Description	Specification	Usage
HDMI Port	J25	Extended Display ports	HDMI port supports up to 4K without HDCP 1.4A spec	External Display
USB 3.1 Type-C	J23	USB 3.1 via USB Type C	USB 3.1 support, HS, SS, including DP alt	USB 3.1 support, HS, SS, including DP alt
LCD Display and Touch connector	J2	100 pin for LCD signals via b2b connector to display adapter board	4-lane MIPI DSI0, DSI1 I2C/SPI/GPIO Backlight	Can work as one dual DSI or both independent display

The Open-Q 835 µSOM development platform can support one of the following display combinations at a time:

Combination 1

HDMI	V2.0 (4K60)
MIPI DSI	2 x 4-lane DSI DPHY 1.2

Combination 2

DP over USB	DisplayPort V1.3 (with the exception of HBR3)
MIPI DSI	2 x 4-lane DSI DPHY 1.2

3.9.5.1 HDMI Connector J25

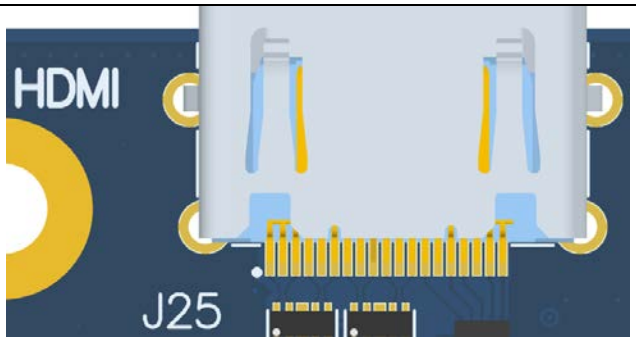


Figure 31 HDMI Type A Connector

The on-board HDMI type A connector enables the Open-Q 835 µSOM development platform to connect to an external HDMI monitor/ television via an HDMI cable. As part of a new feature, the APQ8098 can now support up to 4K UHD (3840 x 2400 at 60fps) and HDMI 2.0 (4K60)/ 4K30 Miracast.

Please note that the Open-Q 835 µSOM Development kit is for evaluation purposes only and may not be HDMI compliant.

3.9.5.2 Display Connector J2

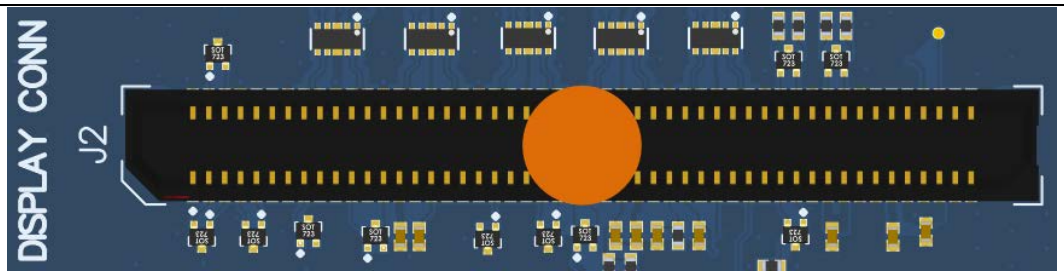


Figure 32 100-Pin Display Connector

The 100-pin display connector provides the following features/ pin-outs which enables the development kit to connect to a MIPI DSI panel/ device:

Note: Please refer to the carrier schematic and display board tech note when designing a custom display board.

- DSI
    - 2 x 4 lane DSI
- Backlight
    - Built-in backlight WLED driver on PMI8998
        - WLED driver supports up to 28.5V output for backlight
    - Primary external backlight (BL0)

        - Backlight control signals
        - External Power
- Display connector – LCD/ AMOLED
    - PMI8998 programmable display bias output voltage:
        - 5V to 6.1V and -1.4V to -6.0V (LCD display)
        - 4.6V to 5V and -1.4V to -5.4V (AMOLED display)
- Additional GPIOs for general purposes available
- VREG_S4A voltage rail from PM8998
    - Required by display for DOVDD
    - 300mA current path
- Touch Panel
    - Supports one touch screen controller
    - Supports I2C or SPI via BLSP12
    - Can chose between I2C or SPI signals in SW U9 via BLSP12

Power specifications

The display connector supports the following power domains:

Display Signal	Power Domain
PM8998 LDO28 (3.3-2.8V)	up to 150 mA
PM8998 LDO14 (1.8V- 2.15V)	up to 150 mA
PM8998 LDO15(1.8V – 2.15V)	up to 300 mA
PM8998 S4A (1.8V)	up to 300 mA
Carrier 3.3V	up to 0.5A
Carrier 5 V	up to 1.5A
Carrier 12 V	up to 0.5A

The Intrinsyc Display Adapter board is an additional PCB that mates with the display connector J2 on the carrier board. This board allows users to interface with the development kit via the LCD that comes preinstalled on the display board. The following figure illustrates the interfacing connectors on the display board.

Note: The display board comes as an additional add-on to the Open-Q 835 µSOM development kit. To purchase this, please visit http://shop.intrinsyc.com or contact Intrinsyc at sales@intrinsyc.com for details.

3.9.5.2.1 CONNECTING THE DISPLAY BOARD TO THE DEVELOPMENT KIT

This configuration allows the user to use the preinstalled LCD display that comes with the display adaptor board. As shown in the block diagram below, the MIPI DSI0 lines, which come from the 100-pin ERM8 connector, directly connects to the LCD panel. See the section below for more details on this LCD panel. It is important to note that connector J1 on the display board needs to connect to J2 on the carrier board for this configuration to work.

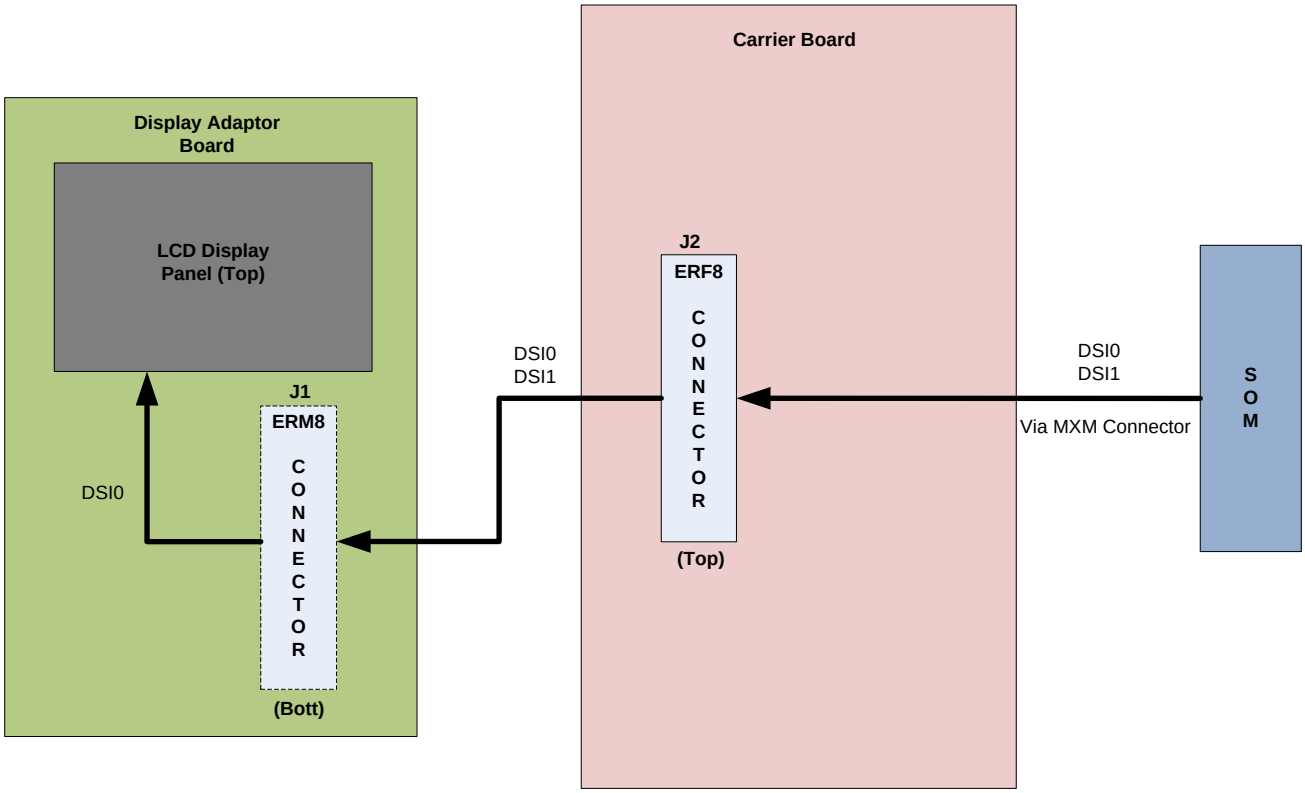


Figure 33 Display Board Default Configuration

3.9.5.2.2 LCD DISPLAY PANEL

Below are the Panel specifications of the preinstalled display panel mounted on the display adaptor board:

- Resolution: 480x854
- LCD Type: IPS
- PCAP touch panel with cover glass
- **No of Lanes:** 1 x 2 lane MIPI DSI interface via Display Board.
- Diagonal Length: 4.5”
- Display Accessory Link: https://shop.intrinsyc.com/products/open-q-810-820-lcd
- Contact sales@intrinsyc.com for more information

Note: The display above is meant to work with the carrier board. Altering the use of this LCD panel is not recommended.

4. ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Ratings

The Development Kit can be powered by either a single cell Li-on battery or by a 12V DC Power via the DC Jack. An external USB-C charger can also be used to charge the battery.

Table 15 Absolute Maximum Input Power Ratings

Parameter	Min	Max	Units
DC power input (DC_IN_JACK), main Carrier Board regulator	-0.3	17	V
Battery Voltage (VBATT)	-0.5	6	V
5V USB VBUS battery charger input voltage source (USB_VBUS)	-0.3	20	V

4.2 Operating Conditions

According to component datasheet values, the operating conditions outline the parameters in which a user can control the behaviour of the development kit. If used within the following conditions, the development kit will meet performance specifications (provided that the absolute maximum ratings have never been exceeded).

Table 16 Operating Conditions

Parameter	Min	Typ	Max	Units
DC power input (DC_IN_JACK), main Carrier Board regulator	+10.8	+12.0	+13.2	V
Battery Voltage (VBATT)	+3.45	+3.8	+4.2	V
5V USB VBUS battery charger input voltage source (USB_VBUS)	+3.6	+5.0	+14	V

4.3 Operating Temperature

The development kit operating temperature ratings listed below are based only on the operating temperature grade of the uSOM and Carrier Board components. Users should consider the specific environmental conditions in which the final product is used in.

Table 17 Operating Temperature

Parameter	Min	Typ	Max	Units
Overall Development Kit	-10	+25	+70	°C